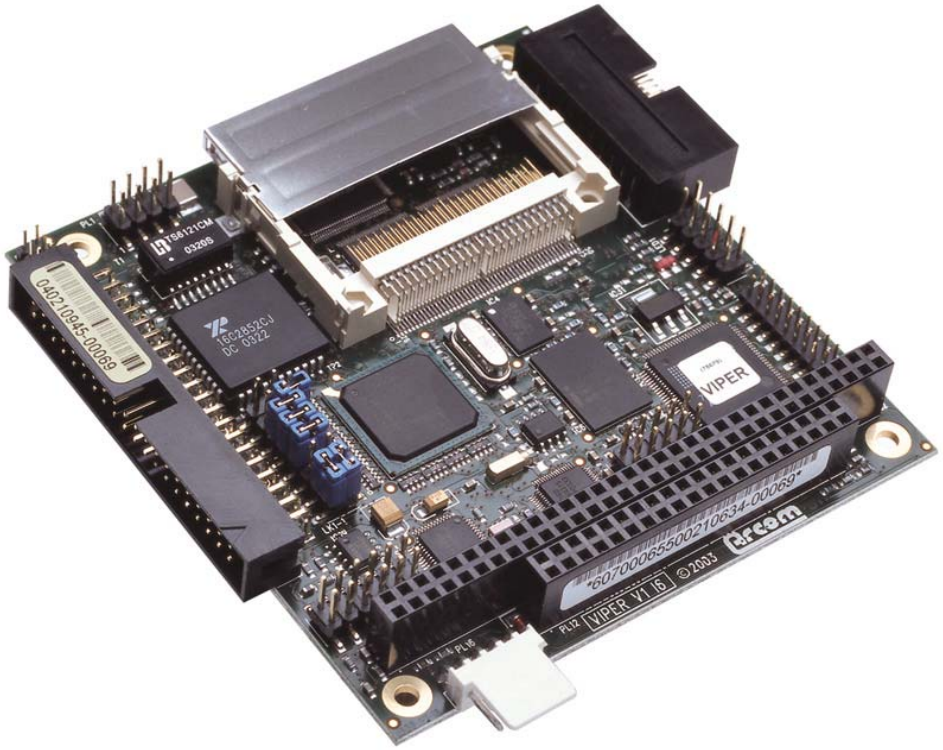
VIPER

Intel PXA255 XScale RISC based PC/104 Single Board Computer

Technical Manual



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Revision History

Manual	*PCB*	*Date*	*Comments*
Issue A	V1 Issue 3	26th June 2003	First full release of Manual
Issue B	V1 Issue 3	8th July 2003	Minor editorial changes
Issue C	V1 Issue 4	14th August 2003	Content update
Issue D	V1 Issue 5	14th October 2003	Minor changes
Issue E	V1 Issue 6	11th December 2003	Update for new PCB Issue
Issue F	V1 Issue 6	11th February 2004	Minor changes
Issue G	V1 Issue 6	14th May 2004	Major technical information enhancements, updated layout
Issue H	V1 Issue 6	15th July 2004	Minor changes

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For contact details, see page 72.

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Contents

Introduction

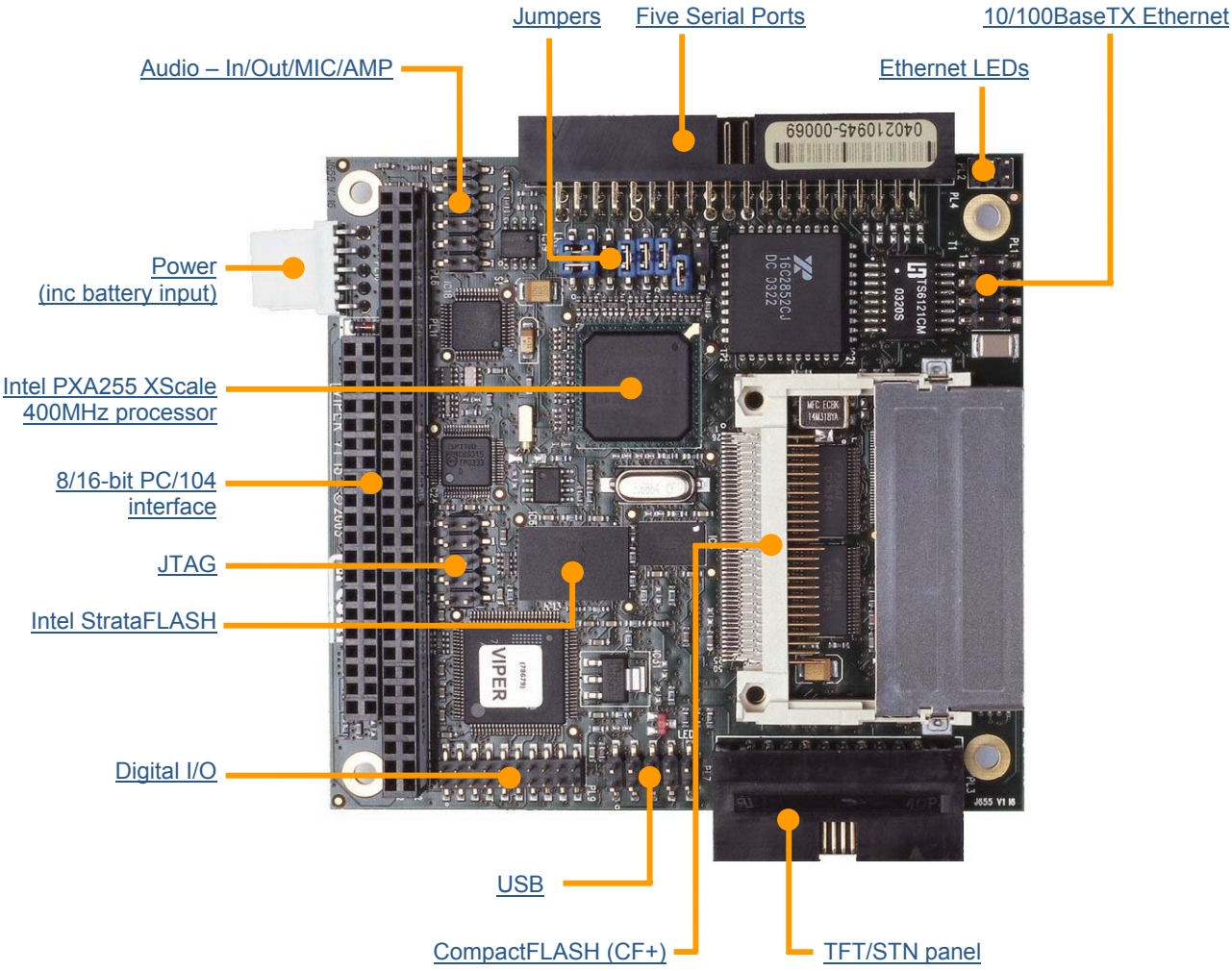
The VIPER is an ultra low power PC/104 compatible single board computer based on the Intel 400MHz PXA255 XScale processor. The PXA255 is an implementation of the Intel XScale micro architecture combined with a comprehensive set of integrated peripherals including, a flat panel graphics controller, DMA controller, interrupt controller, real time clock and multiple serial ports. The VIPER board offers a wide range of features making it ideal for power sensitive embedded communications and multimedia applications.

The board is available in the following standard variants:

- VIPER-400-M64-F32: Intel XScale ™ PXA255 400MHz microprocessor, 64MByte SDRAM, 32MByte FLASH.
- VIPER-400-M64-F16: Intel XScale ™ PXA255 400MHz microprocessor, 64MByte SDRAM, 16MByte FLASH.
- VIPER-400-M64-F32-I: Intel XScale ™ PXA255 400MHz microprocessor, 64MByte SDRAM, 32MByte FLASH, Industrial temperature range.
- VIPER-400-M64-F16-I: Intel XScale ™ PXA255 400MHz microprocessor, 64MByte SDRAM, 16MByte FLASH, Industrial temperature range.

For alternative memory configurations, please contact Arcom.

VIPER 'at a glance'



VIPER features

Microprocessor

- Intel XScale™ PXA255 400MHz RISC processor

Cache

- 32K data cache, 32K instruction cache, 2K mini data cache

System memory

- Up to 64MByte un-buffered 3.3V SDRAM

Silicon disk

- Up to 32MByte Intel Strata FLASH (with FLASH access LED)
- 1MByte Bootloader FLASH EPROM (with FLASH access LED)
- 256KByte SRAM (with external battery backup)
- Type I/II CompactFLASH (CF+) socket

Video

- TFT/STN (3.3V or 5V – factory fit) flat panel graphics controller
- Up to 800X600 resolution
- 8/16bpp
- Backlight Control

Audio

- National Semiconductor A AC'97 CODEC (16bit) and LM4880 Power Amp
- Line IN, Line OUT, Microphone and 250mW per channel amplified output

Serial ports

- 5 x 16550 compatible high-speed UARTs
- 4 x RS232 and 1 x RS422/485 Interfaces
- 2 x channels with 128Byte Tx/Rx FIFO

USB host interface

- Two USB 1.1 compliant interfaces
- Short circuit protection and 500mA current limit protection

Network support

- SMSC LAN91C111 10/100BaseTX Ethernet controller
- One 10/100BaseTX NIC port

Real Time Clock (RTC)

- Battery backed RTC (external battery)
- ± 1minute/month accuracy, at 25°C.

Watchdog

- Adjustable timeout of 271ns to 19 minutes, 25 seconds

General Purpose I/O (GPIO)

- 8 x 5V tolerant Inputs
- 8 x 3.3V Outputs (5V tolerant)

User configuration

- 1 user-configurable jumper

Expansion

- PC/104 expansion bus - 8/16 bit ISA bus compatible interface

JTAG port

- Download data to FLASH memory
- Debug and connection to In-Circuit Emulator (ICE)

Power

- Typically 2W from a single 5V supply
- Power Management features allowing current requirements to be as low as 107mA ±5mA (535mW ±25mW).

Size

- PC/104 compatible footprint 3.8” x 3.6” (96mm x 91mm)

VIPER support products

The VIPER is supported by the following products:

- **VIPER-UPS (Uninterruptible Power Supply)**
  The VIPER-UPS serves as a 5V DC power supply and battery back up system for the VIPER. The UPS accepts between 10 – 36 VDC (10-25VAC) input and generates the +5V supply for the VIPER. In addition to this, it includes an intelligent battery charger/switch capable of using either the onboard 500mAHr NiMH battery or an external sealed lead acid rechargeable battery. For further details, see www.arcom.com/products/icp/pc104/processors/viper_UPS.htm.

- **VIPER-ICE (Industrial Compact Enclosure)**
  The VIPER-ICE is a simple low cost aluminum enclosure, which provides easy connection to all on board features. The enclosure includes the VIPER-UPS and optionally a color Q-VGA (320x240) TFT flat panel display and analog touch screen.

- **VIPER-FPIF1 (Flat Panel Interface)**
  The VIPER-FPIF1 is a simple board that enables easy connection between the VIPER and an LCD flat panel. See section VIPER-FPIF1 details, page 33 for further details. Contact Arcom (see Appendix A – Contacting Arcom, page 72) for purchasing information.

Handling your board safely

Anti-static handling

This board contains CMOS devices that could be damaged in the event of static electricity discharged through them. At all times, please observe anti-static precautions when handling the board. This includes storing the board in appropriate anti-static packaging and wearing a wrist strap when handling the board.

Packaging

Please ensure that should a board need to be returned to Arcom, it is adequately packed, preferably in the original packing material.

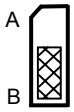
Electromagnetic compatibility (EMC)

The VIPER is classified as a component with regard to the European Community EMC regulations and it is the users responsibility to ensure that systems using the board are compliant with the appropriate EMC standards.

Conventions

Symbols

The following symbols are used in this guide:

Symbol	Explanation
	Note - information that requires your attention.
	Tip - a handy hint that may provide a useful alternative or save time.
	Caution – proceeding with a course of action may damage your equipment or result in loss of data.
	Jumper fitted on pin A.
	Jumper fitted on pin B.
	Jumper is fitted.
	Jumper is not fitted.

Tables

With tables such as that shown below, the white cells show information relevant to the subject being discussed. Grey cells are not relevant in the current context.

Byte lane	Most Significant Byte								Least Significant Byte							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	-	-	-	-	-	-	-	RETRIG	AUTO CLR	R_DIS
Reset	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0

Relevant information

Getting started

Depending on the Development Kit purchased, a Quickstart Manual is provided for Windows CE .NET, embedded Linux, or VxWorks to enable users to set-up and start using the board. Please read the relevant manual and follow the steps defining the set-up of the board. Once you have completed this task you will have a working VIPER system and can start adding further peripherals enabling development to begin.

This section provides a guide to setting up and using of some of the features of the VIPER. For more detailed information on any aspect of the board see Detailed hardware description, page 13.

Using the VIPER

Using the CompactFLASH™ socket

The VIPER is fitted with a Type I/II CompactFLASH socket mounted on the topside of the board. The socket is connected to Slot 0 of the PXA255 PC Card interface. It supports 3.3V Type I and II CompactFLASH cards, for both memory and IO. The VIPER supports hot swap changeover of the cards and notification of card insertion.

RedBoot supports ATA type CompactFLASH cards. Files can be read providing the card is formatted with an EXT2 file system. Eboot cannot boot from CompactFlash.

5V CompactFLASH is not supported.

The CompactFLASH card can only be inserted one way into the socket. The correct orientation is for the top of the card, i.e. with the normal printed side face down to the PCB.

Using the serial interfaces (RS232/422/485)

The five serial port interfaces on the VIPER are fully 16550 compatible. Connection to the serial ports is made via a 40-way boxed header. The pin assignment of this header has been arranged to enable 9-way IDC D-Sub plugs to be connected directly to the cable. See the section PL4 – COMS ports, page 63, for pin assignment and connector details.

A suitable cable for COM1 is provided as part of the Development Kit. The D-Sub connector on this cable is compatible with the standard 9-way connector on a desktop computer.

Using the audio features

There are four audio interfaces supported on the VIPER: amp out, line out, line in and microphone. The line in, line out and amp interfaces support stereo signals and the microphone provides a mono input. The amplified output is suitable for driving an 8Ω load with a maximum power output of 250mW per channel. Connections are routed to PL6 - see the sections Audio (page 38) and PL6 – Audio connector (page 65) for further connector details.

Using the USB ports

The standard USB connector is a 4-way socket, which provides power and data signals to the USB peripheral. The 10-way header PL7 has been designed to be compatible with PC expansion brackets that support two USB sockets. See the sections USB interface (page 42) and PL7 – USB connector (page 65) for further details.

Using the Ethernet interface

The SMSC LAN91C111 10/100BaseTX Ethernet controller is configured by the RedBoot bootloader for embedded Linux or VxWorks, and by Windows CE .NET once it has booted. Connection is made via connector PL1. A second connector PL2 provides activity and link status outputs for control LED's. See the sections 10/100BaseTX Ethernet (page 43), PL1 – 10/100BaseTX Ethernet connector (page 61) and PL2 – Ethernet status LED's connector (page 61) for further details.

Using the PC/104 expansion bus

PC/104 modules can be used with the VIPER to add extra functionality to the system. This interface supports 8/16 bit ISA bus style peripherals.

Arcom has a wide range of PC/104 modules, which are compatible with the VIPER. These include modules for digital I/O, analog I/O, motion control, video capture, CAN bus, serial interfaces, etc. Please contact the Arcom sales team if a particular interface you require does not appear to be available as these modules are in continuous development. Contact details are provided in Appendix A – Contacting Arcom, page 72.

In order to use a PC/104 board with the VIPER it should be plugged into PL11 for 8-bit cards and PL11/PL12 for 8/16-bit cards. See the sections PC/104 interface (page 48) and PL11 & PL12 – PC/104 connectors (page 67) for further details.

Before powering up the system, check that the jumper settings on the card for I/O address and IRQ settings do not conflict with any devices on the VIPER. The ISA interface on the VIPER does not support DMA. See the section Interrupt assignments, page 25, for details about PC/104 interrupt use.

The VIPER provides +5V to a PC/104 add-on-board via the PL11 and PL12 connectors. If a PC/104 add-on-board requires a +12V supply, then +12V must be supplied to the VIPER Power Connector PL16 pin 4. If –12V or –5V are required, these must be supplied directly to the PC/104 add-on board.

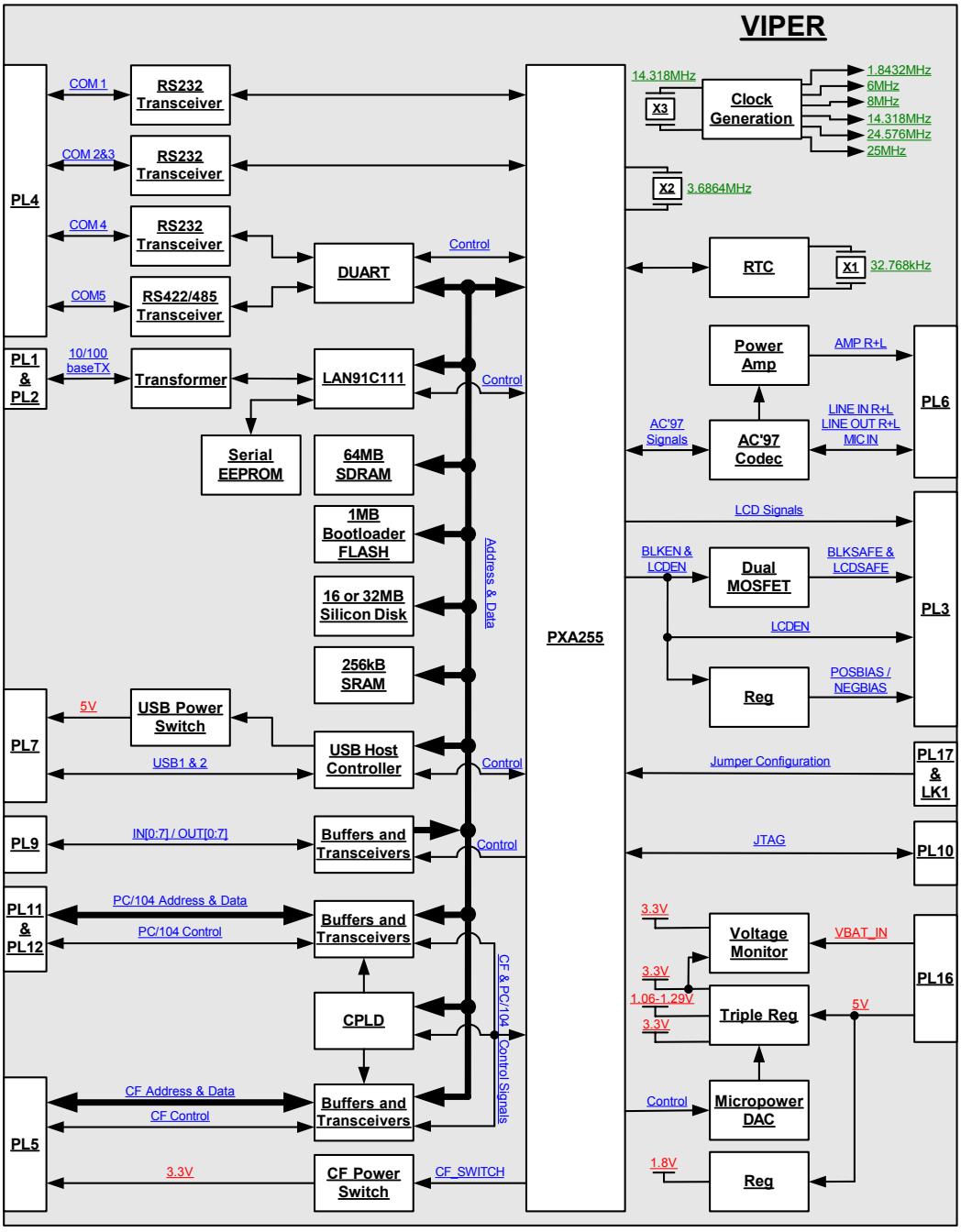
The VIPER is available with non-stack through connectors by special order. Contact Arcom (see Appendix A – Contacting Arcom, page 72) for more details.

Detailed hardware description

The following section provides a detailed description of the functions provided by the VIPER. This information may be required during development after you have started adding extra peripherals or are starting to use some of the embedded features.

VIPER block diagram

The diagram below illustrates the functional organization of the VIPER PC/104 SBC.



VIPER address map

PXA255 chip select	Physical address	Bus/register width	Description
-	0xA4000000 – 0xFFFFFFFF	-	Reserved
SDCS0	0xA0000000 – 0xA3FFFFFC	32-bit	SDRAM, IC2&3
-	0x4C000000 – 0x9FFFFFFF	-	Reserved
NA	0x48000000 – 0x4BFFFFFF	32-bit	Memory Control Registers [1]
NA	0x44000000 – 0x47FFFFFF	32-bit	LCD Control Registers [1]
NA	0x40000000 – 0x43FFFFFF	32-bit	PXA255 Peripherals [1]
-	0x3C200400 – 0x3FFFFFFF	-	Reserved
NA	0x3C000000 – 0x3C1FFFFF	16-bit	PC/104 Memory Space
-	0x30000400 – 0x3BFFFFFF	-	Reserved
NA	0x30000000 – 0x300003FF	16-bit	PC/104 I/O Space
NA	0x20000000 – 0x2FFFFFFF	32-bit	CompactFLASH, PL5
-	0x14840000 – 0x1FFFFFFF	-	Reserved
CS5	0x14800000 – 0x1483FFFF	8-bit	SRAM (see page 24)
-	0x14500001 – 0x47FFFFFF	-	Reserved
CS5	0x14500000 – 0x14500000	8-bit	General Purpose Input, PL9 (see page 66)
-	0x14300020 – 0x144FFFFF	-	Reserved
CS5	0x14300010 – 0x1430001F	8-bit	COM4 (see page 46)
CS5	0x14300000 – 0x1430000F	8-bit	COM5 (see page 46)
-	0x14100004 – 0x142FFFFF	-	Reserved
CS5	0x14100002 – 0x14100003	8-bit	ICR Register (see page 26)
CS5	0x14100000 – 0x14100001	8-bit	PC104I Register (see page 26)
-	0x10000004 – 0x140FFFFF	-	Reserved
CS4	0x10000000 – 0x10000002	32-bit	Ethernet Data port
-	0x0C000004 – 0x0FFFFFFF	-	Reserved
CS3	0x0C000000 – 0x0C000002	16-bit	USB Host Controller
-	0x08000310 – 0x0BFFFFFF	-	Reserved
CS2	0x08000300 – 0x0800030E	16-bit	Ethernet I/O Space
-	0x06000000 – 0x080002FF	-	Reserved
CS1	0x04000000 – 0x05FFFFFE	16-bit	FLASH Memory / Silicon Disk
-	0x00100000 – 0x03FFFFFF	-	Reserved
CS0	0x00000000 – 0x000FFFFE	16-bit	Bootloader FLASH

[1] Details of the internal registers are in the Intel Developer Manual on the Development Kit CD.

Translations made by the MMU

For details of translations made by the MMU by Redboot for embedded Linux, please refer to VIPER embedded Linux Quickstart Manual.

For details of translations made by the MMU by Redboot for VxWorks, please refer to VIPER VxWorks Quickstart and Technical Manual

For details of translations made by the MMU for Windows CE .NET, please check the Windows CE .NET documentation for more information about memory mapping. One source of this information is on the msdn website under *Windows CE .NET Memory Architecture*.

PXA255 processor

The PXA255 is a low power ARM (version 5TE) instruction set compliant RISC processor. The PXA255 does not include a floating-point unit. The device does, however, contain a DSP co-processor to enhance multimedia applications.

The 400MHz PXA255 is driven by a 3.6864 MHz clock, which generates all the high-speed clocks within the device. The default run mode frequency is 400MHz for embedded Linux, VxWorks and Windows CE .NET. Currently embedded Linux and VxWorks supports changing the operating frequency and Windows CE .NET will provide support shortly. Please refer to the relevant operating system technical manual to select an alternative operating frequency.

The processor has two supply inputs: I/O and core generated on the VIPER from the main +5V supply input. The I/O supply is powered from +3.3V, and the core is powered from a +1.06 to +1.3V adjustable supply. See the section Processor power management, page 55, for operation details.

The PXA255 has an integrated Memory and CompactFlash Controller with 100 MHz Memory Bus, 32 KB data and 32 KB instruction caches and 2 KB Mini data cache for streaming data.

The PXA255 provides up to 85 GPIO pins, many of these have been configured for alternative functions like the AC'97 and PC card / CompactFLASH interfaces. Details of these pin configurations are provided in the section PXA255 GPIO pin assignments, page 17.

The PXA255 also has the following features that can be used on the VIPER:

- Peripheral Control Module:
  - 16 channel configurable DMA controller.
  - Integrated LCD controller with unique DMA for fast color screen support.
  - Serial ports including AC'97, three UARTs, and enhanced USB end point interface.

- System Control Module:
  - General-purpose interruptible I/O ports.
  - Real-time clock.
  - Watchdog.
  - Interval timers.
  - Power management controller.
  - Interrupt controller.
  - Reset controller.
  - Two on-chip oscillators.

The PXA255 processor is packaged in a 256-pin PBGA, which is attached to the board during the assembly process.

The PXA255 processor is a low power device and does not require a heat sink for temperatures up to 70°C (85°C for the industrial variant).

PXA255 GPIO pin assignments

The following table summarizes the use of the 85 PXA255 GPIO pins, their direction, alternate function and active level.

For embedded Linux the GPIO pins are setup by Redboot. Under VxWorks and Windows CE .NET, they are setup by themselves and not by the bootloader.

Key:

AF Alternate function.
Dir Pin direction.
Active Function active level or edge.
Sleep Pin state during sleep mode (all Hi-Z states are to '1' during sleep).

GPIO No	AF	Signal Name	Dir	Active	Sleep	Function	See section...
0	0	ETHER_INT	Input	↑	Input	Ethernet Interrupt	
1	0	PC/104_IRQ	Input	See page 26	Input	CPLD Interrupt	Interrupt assignments (page 25) and Wake up events (page 58)
2	0	USB_IRQ	Input	↓	Input	USB Interrupt	
3	0	UART_INT1	Input	↑	Input	COM 5 Interrupt	
4	0	UART_INT2	Input	↑	Input	COM 4 Interrupt	
5	0	USER_CONFIG1	Input	NA	Input	User Config 1, Jumper LK2	User configurable jumper 1 – LK2 (page 70)
6	0	PSU_DATA	Output	NA	0	Microprocessor Core Voltage DAC Data	Processor power management (page 55)
7	0	Reserved	Input	NA	Input	Reserved	Reserved – LK3 (page 70)
8	0	CF_RDY	Input	NA	Input	CompactFLASH Ready/nBusy	Interrupt assignments, (page 25 and CompactFLASH page 24)
9	0	BLKEN	Output	High	0	LCD Backlight Enable	LCD backlight enable (page 31)
10	0	LCDEN	Output	High	0	LCD Logic Supply Enable	LCD logic supply enable (page 32)
11	0	PSU_CLK	Output	↑	0	Microprocessor Core Voltage DAC Clock	Processor power management (page 55)
12	0	SHDN	Output	High	1	COM 1, 2, 3 & 4 UART Shutdown	UART power management (page 57)
13	0	EN1#	Output	Low	0	COM 1, 2, 3 & 4 UART Enable	

GPIO No	AF	Signal Name	Dir	Active	Sleep	Function	See section...
14	0	FLASH_ STATUS	Input	NA	Input	Bootloader FLASH Status, Ready / nBusy	Interrupt assignments (page 25) and FLASH memory/silicon disk (page 23)
15	2	CS1	Output	Low	Hi-Z	Chip Select 1	VIPER address map (page 14)
16	2	PWM0	Output	See inverter datasheet	0	Backlight Brightness On/Off or variable if PWM	LCD backlight brightness control (page 32)
17	2	PWM1	Output	NA	0	STN Bias	STN BIAS voltage (page 32)
18	1	ARDY	Input	Low	Input	10/100 Ethernet PHY Ready	-
19	0	PSU_nCS_LD	Output	Low	0	Microprocessor Core Voltage DAC Chip Select	Processor power management (page 55)
20	0	OUT0	Output	User Config	0	User Config	General purpose I/O (page 39)
21	0	OUT1					
22	0	OUT2					
23	0	OUT3					
24	0	OUT4					
25	0	OUT5					
26	0	OUT6					
27	0	OUT7					
28	1	AC97_BITCLK	Input	↑	Input	BITCLK	-
29	1	AC97_IN	Input	NA	Input	SDATA_IN0	
30	2	AC97_OUT	Output	NA	0	SDATA_OUT	
31	2	AC97_SYNC	Output	↑	0	SYNC	
32	0	CF_DETECT	Input	↓	Input	CF Detection	Interrupt assignments (page 25) and CompactFLASH (page 24)
33	2	CPLDCS	Output	Low	Hi-Z	Chip Select 5	VIPER address map, (page 14)

GPIO No	AF	Signal Name	Dir	Active	Sleep	Function	See section...
34	1	RXD1	Input	NA	Input	COM1 Receive Data	
35	1	CTS1	Input	NA	Input	COM1 Clear To Send	
36	1	DCD1	Input	NA	Input	COM1 Data Carrier Detect	
37	1	DSR1	Input	NA	Input	COM1 Data Sender Ready	
38	1	RI1	Input	NA	Input	COM1 Ring Indicator	
39	2	TXD1	Output	NA	0	COM1 Transmit Data	
40	2	DTR1	Output	NA	0	COM1 Data Terminal Ready	Serial COMs ports (page 45) and **PL4 – COMS ports** (page **63**).
41	2	RTS1	Output	NA	0	COM1 Request To Send	
42	1	RXD2	Input	NA	Input	COM2 Receive Data	
43	2	TXD2	Output	NA	0	COM2 Transmit Data	
44	1	CTS2	Input	NA	Input	COM2 Clear To Send	
45	2	RTS2	Output	NA	0	COM2 Request To Send	
46	2	RXD3	Input	NA	Input	COM3 Receive Data	
47	1	TXD3	Output	NA	0	COM3 Transmit Data	
48	2	CB_POE	Output	Low	Hi-Z	Socket 0 & 1 Output Enable	
49	2	CB_PWE	Output	Low	Hi-Z	Socket 0 & 1 Write Enable	
50	2	CB_PIOR	Output	Low	Hi-Z	Socket 0 & 1 I/O Read	-
51	2	CB_PIOW	Output	Low	Hi-Z	Socket 0 & 1 I/O Write	
52	2	CB_PCE1	Output	Low	Hi-Z	Socket 0 & 1 Low Byte Enable	
53	2	CB_PCE2	Output	Low	Hi-Z	Socket 0 & 1 High Byte Enable	
54	2	CB_PKTSEL	Output	NA	0	PSKTSEL 0 = Socket 0 Select / 1 = Socket 1 Select	-
55	2	CB_PREG	Output	Low	0	PREG	-
56	1	CB_PWAIT	Input	Low	Input	PWAIT	-
57	1	CB_PIOIS16	Input	Low	Input	IOIS16	

GPIO No	AF	Signal Name	Dir	Active	Sleep	Function	See section...
58	2	LCD_D0	Output	NA	0	LCD Data Bit 0	
59	2	LCD_D1	Output	NA	0	LCD Data Bit 1	
60	2	LCD_D2	Output	NA	0	LCD Data Bit 2	
61	2	LCD_D3	Output	NA	0	LCD Data Bit 3	
62	2	LCD_D4	Output	NA	0	LCD Data Bit 4	
63	2	LCD_D5	Output	NA	0	LCD Data Bit 5	
64	2	LCD_D6	Output	NA	0	LCD Data Bit 6	
65	2	LCD_D7	Output	NA	0	LCD Data Bit 7	
66	2	LCD_D8	Output	NA	0	LCD Data Bit 8	
67	2	LCD_D9	Output	NA	0	LCD Data Bit 9	
68	2	LCD_D10	Output	NA	0	LCD Data Bit 10	Flat panel display support (page 29) and PL3 – LCD connector (page 62)
69	2	LCD_D11	Output	NA	0	LCD Data Bit 11	
70	2	LCD_D12	Output	NA	0	LCD Data Bit 12	
71	2	LCD_D13	Output	NA	0	LCD Data Bit 13	
72	2	LCD_D14	Output	NA	0	LCD Data Bit 14	
73	2	LCD_D15	Output	NA	0	LCD Data Bit 15	
74	2	LCD_FCLK	Output	NA	0	LCD Frame Clock (STN) Vertical Sync (TFT)	
75	2	LCD_LCLK	Output	NA	0	LCD Line Clock (STN) / Horizontal Sync (TFT)	
76	2	LCD_PCLK	Output	NA	0	LCD Pixel Clock (STN) / Clock (TFT)	
77	2	LCD_BIAS	Output	NA	0	LCD Bias (STN) / Date Enable (TFT)	
78	2	ETHERCS2	Output	Low	Hi-Z	Chip Select 2	VIPER address map (page 14)
79	2	USBCS	Output	Low	Hi-Z	Chip Select 3	
80	2	ETHERCS1	Output	Low	Hi-Z	Chip Select 4	
81	0	SDRAM	Input	NA	Input	SDRAM Size Detection 0 = 64MB, 1 = 16MB	-
82	0	CF_SWITCH	Output	High	0	CompactFLASH Power Switch Enable	CompactFLASH (page 24) and CompactFLASH power management (page 57)
83	0	RTC_IO	Bidirec-tional	NA	0	RTC Data	Real Time Clock (page 21)
84	0	RTC_CLK	Output	↓	0	RTC Clock	

Real Time Clock

There are two RTCs on the VIPER: Under embedded Linux and VxWorks the internal RTC of the PXA255 should only be used for power management events, and an external Dallas DS1307 RTC should be used to keep the time and date. Under Windows CE .NET the time and date stamps are copied from the external RTC to the internal RTC of the PXA255, to run the RTC internally.

The accuracy of the DS1307 RTC is based on the operation of the 32.768KHz watch crystal. Its calibration tolerance is ±20ppm, which provides an accuracy of +/-1 minute per month if the board is in an ambient environment of +25°C. When the board is operated outside this temperature then the accuracy may be degraded by -0.035ppm/°C² ±10% typical. The watch crystal's accuracy will age by ±3ppm max in the first year, then ±1ppm max in the year after, and logarithmically decreasing in subsequent years.

The following PXA255 GPIO pins are used to emulate the I²C interface to the DS1307 RTC:

PXA255 Pin	Function
GPIO84	Clock (100MHz max)
GPIO83	Data

The DS1307 RTC also contains 64Bytes of RAM, which can be used for any user data that needs to be recoverable on power-up.

To ensure the DS1307 RTC doesn't lose track of the date and time when the 5V supply is powered-down, an external battery must be fitted. See the section Battery backup, page 51, for details.

Watchdog timer

The PXA255 contains an internal watchdog timer, which can be used to protect against erroneous software. Timeout periods can be adjusted from 271ns to 19 minutes 25 seconds. When a timeout occurs the board is reset. On reset the watchdog timer is disabled until enabled again by software.

For further details see the Arcom operating system Technical Manual and the Intel PXA255 developer's manual on the Development Kit CD.

Memory

The VIPER has four types of memory fitted:

- 1MByte of bootloader FLASH containing Redboot to boot embedded Linux or VxWorks, or Eboot to boot Windows CE .NET.
- A resident FLASH disk containing the OS and application images.
- SDRAM for system memory.
- 256KBytes of Static RAM (SRAM).

Bootloader FLASH

A 1MByte Bottom Boot FLASH EPROM device, arranged as 512Kbit x 16, is used as the bootloader FLASH. It holds Redboot (for embedded Linux or VxWorks) or Eboot (for Windows CE .NET), together with configuration information. When the microprocessor comes out of reset it boots the relevant bootloader from here, which in turn boots up the OS from the FLASH memory/silicon disk. Whenever the Bootloader FLASH memory is accessed the FLASH access LED illuminates.

FLASH memory/silicon disk

The VIPER supports 16MBytes or 32MBytes of Intel StrataFLASH memory for the OS and application images. The FLASH memory is arranged as 64Mbit x 16-bits (16MByte device) or as 128Mbit x 16-bits (32MByte device) respectively.

The FLASH memory array is divided into equally sized symmetrical blocks that are 64-Kword in size. A 128Mbit device contains 128 blocks, and 256Mbit device contains 256 blocks. Flash cells within a block are organized by rows and columns. A block contains 512 rows by 128 words. The words on a row are divided into 16 eight-word groups.

The PXA255 GPIO14 pin is connected to the FLASH memory status output. This pin can be used to generate an interrupt to indicate the completion of a CFI command.

Whenever the FLASH memory is accessed the FLASH access LED illuminates.

SDRAM interface

There are two memory configurations supported by the VIPER: 16MBytes or 64MBytes of SDRAM located in Bank 0. The SDRAM is configured as 4MBytes x 32-bits (16MBytes) or 16MBytes x 32-bits (64MBytes), by 2 devices with 4 internal banks of 1MBytes or 4MBytes x 16-bits.

These are surface mount devices soldered to the board and cannot be upgraded. RedBoot (embedded Linux and VxWorks) automatically detects the amount of memory fitted to the board, and configures the SDRAM controller accordingly. For Windows CE .NET applications the SDRAM memory will always be 64MBytes.

The SDRAM controller supports running the memory at frequencies between 50MHz and 99.5MHz (default). This can be configured to achieve the optimum balance between power consumption and performance.

Static RAM

The VIPER has a 256KByte SRAM device fitted, arranged as 256Kbit x 8-bits. Access to the device is on 16-bit boundaries, whereby the least significant byte is the SRAM data and the 8-bits of the most significant byte are don't care bits. The reason for this is that the PXA255 is not designed to interface to 8-bit peripherals. This arrangement is summarized in the following data bus table:

Most Significant Byte								Least Significant Byte							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Don't Care								SRAM Data							

The data in the SRAM can be made non-volatile by fitting an external battery to power the device in the event of power loss on the main VIPER 5V supply. See the section Battery backup page 51 for details.

CompactFLASH

The CompactFLASH connector PL5 is interfaced to Slot 0 of the PXA255 PC card controller, and appears in PC card memory space socket 0.

This is a hot swappable 3.3V interface, controlled by the detection of a falling edge on GPIO32 when a CompactFLASH card has been inserted. On detection set GPIO82 to logic '1' to enable the 3.3V supply to the CompactFLASH connector. The CompactFLASH (RDY/nBSY) signal interrupts on GPIO8.

Address	Region Name
0x2C000000 – 0x2FFFFFFF	Socket 0 Common Memory Space
0x28000000 – 0x2BFFFFFF	Socket 0 Attribute Memory Space
0x24000000 – 0x27FFFFFF	Reserved
0x20000000 – 0x23FFFFFF	Socket 0 I/O Space

Interrupt assignments

Internal interrupts

For details on the PXA255 interrupt controller and internal peripheral interrupts please see the Intel PXA255 developer's manual on the Development Kit CD.

External interrupts

The following table lists the PXA255 signal pins used for generating external interrupts.

PXA255 Pin	Peripheral	Active
GPIO0	Ethernet	
GPIO1	PC/104 interrupt controller	See PC/104 interrupts, page 26
GPIO2	USB	
GPIO3	COM5	
GPIO4	COM4	
GPIO8	CompactFLASH RDY/nBSY	Ready =  , Busy = 
GPIO14	FLASH (OS)	Ready =  , Busy = 
GPIO32	CompactFLASH card detect	

PC/104 interrupts

The PC/104 interrupts are logically OR'ed together so that any interrupt generated on the PC/104 interface generates an interrupt input on GPIO1.

The PC/104 interrupting source can be identified by reading the PC104I register located at offset 0x100000 from CS5 (0x14000000). The register indicates the status of the interrupt lines at the time the register is read. The relevant interrupt has its corresponding bit set to '1'. The PXA255 is not designed to interface to 8-bit peripherals, so only the least significant byte from the word contains the data.

PC/104 interrupt register [PC104I]

Byte lane	Most Significant Byte								Least Significant Byte							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	-	-	IRQ12	IRQ11	IRQ10	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3
Reset	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0
R/W	-	-	-	-	-	-	-	-	R/W							
Address	0x14100000															

PC/104 interrupts IRQ9, IRQ14 and IRQ15 are not used by the VIPER, please use an alternate interrupt source from the table above.

The ICR Register located at offset 0x100002 from CS5 (0x14000000) must be set-up correctly for the OS running. The PC/104 interrupts are signaled and handled slightly differently between embedded Linux / VxWorks and Windows CE .NET. See the following relevant subsections for specific PC/104 details for the target OS.

Interrupt configuration and reset register [ICR]

Byte lane	Most Significant Byte								Least Significant Byte							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	-	-	-	-	-	-	-	R_DIS	AUTO_CLR	RETRIG
Reset	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0
R/W	-	-	-	-	-	-	-	-	W							
Address	0x14100002															

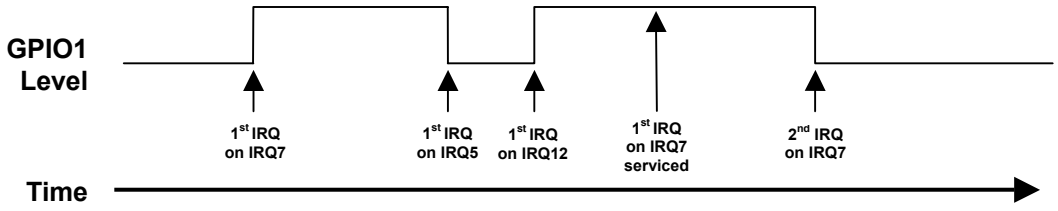
ICR Bit Functions

Bit	Name	Value	Function
0	RETRIG	0	No interrupt retrigger (embedded Linux and VxWorks).
		1	Interrupt retrigger (Windows CE .NET).
1	AUTO_CLR	0	No auto clear interrupt / Toggle GPIO1 on new interrupt.
		1	Auto clear interrupt / Low to high transition on GPIO1 on First Interrupt.
2	R_DIS	0	Keep set as 0 under normal operating conditions. See the section Power management, page 52 for details.
		1	
3 - 7	-	X	No function.

PC/104 interrupts under embedded Linux and VxWorks

Leave the ICR register set to its default value, so that a new interrupt causes the microprocessor PC/104 interrupt pin GPIO1 to be toggled for every new interrupt on a different PC/104 interrupt source. Ensure the GPIO1 input is set up in a level triggered mode. The retrigger interrupt function is not required for embedded Linux or VxWorks.

The following diagram gives an example of how the PC/104 interrupt on GPIO1 behaves over time when the ICR AUTO_CLR bit is set to '0':



Once the VIPER microprocessor has serviced a PC/104 interrupt, clear the corresponding bit in the PC104I register by writing '1' to it.

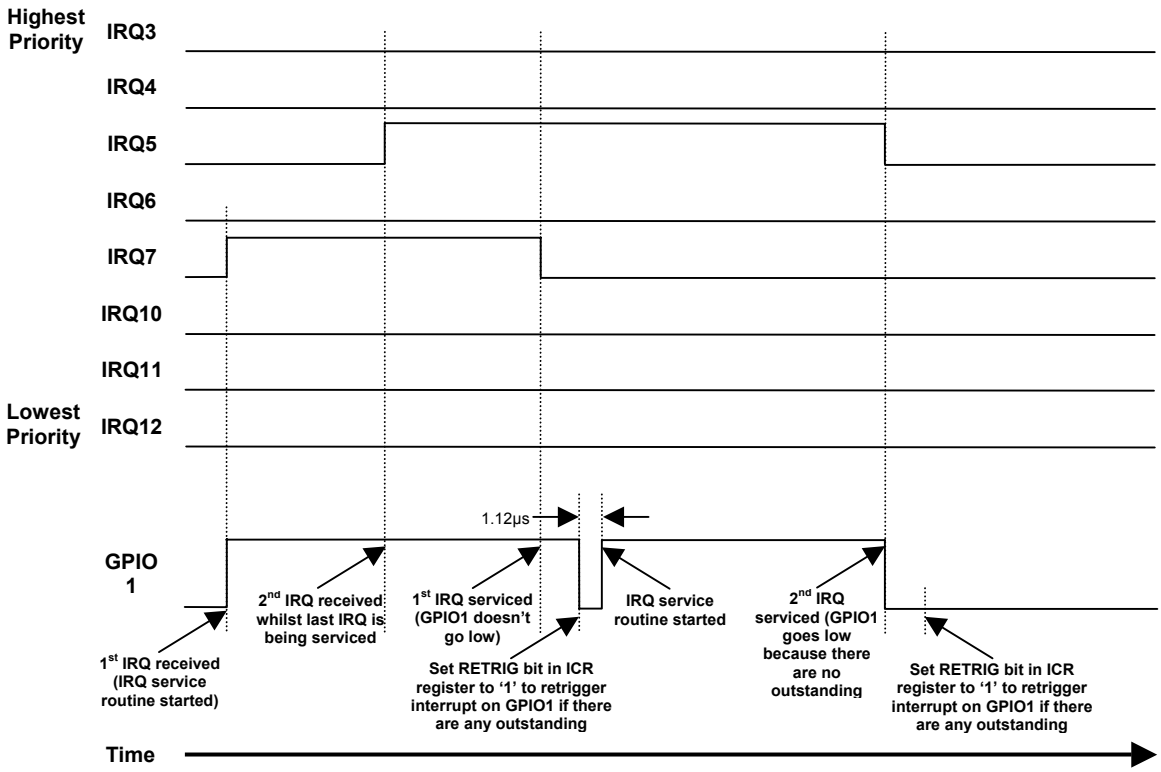
PC/104 interrupts under Windows CE .NET

Write 0x2 to the ICR Register so that the first PC/104 interrupt source causes the PXA255 PC/104 interrupt pin GPIO1 to receive a low to high transition. When the first PC/104 interrupt occurs the Interrupt service routine will start polling through the PC/104 interrupt sources in the PC104I register. The first bit it sees set to a '1', sets a semaphore to make a program run to service the corresponding interrupt.

Once this program has serviced the interrupt the interrupting source returns its interrupt output to the inactive state ('0') if it hasn't requested another interrupt whilst the microprocessor serviced the last interrupt. Once this happens the corresponding bit in the PC104I register shall be automatically cleared. Each PC/104 board requesting an interrupt shall keep its interrupt in the active state ('1') until the interrupt has been serviced by the microprocessor. When there are no interrupts outstanding the level of the PC/104 interrupt on GPIO1 shall automatically return to logic '0'. If it is still '1' then there are interrupts outstanding, which would have occurred during the servicing of the last interrupt.

To capture any interrupts that could have occurred whilst the last interrupt was serviced, the retrigger interrupt bit in the ICR register is set to '1' to retrigger a low to high transition on GPIO1 to restart the interrupt polling mechanism if there are any outstanding interrupts.

The diagram below explains how the PC/104 interrupt on GPIO1 behaves over time when the ICR AUTO_CLR bit is set to '1':



Flat panel display support

The Intel PXA255 processor contains an integrated LCD display controller that permits 1, 2, and 4-bit gray-scale, and 8 or 16-bit color pixels. A 256-byte palette RAM provides flexible color mapping capabilities. The LCD display controller supports active (TFT) and passive (STN) LCD displays.

The PXA255 can drive displays with a resolution up to 800x600, but as there is a unified memory structure, the bandwidth to the application decreases significantly. If the application makes significant use of memory, such as when video is on screen, you may also experience FIFO under-run to the LCD causing the frames rates to drop or display image disruption. Reducing the frame rate to the slowest speed possible gives the maximum bandwidth to the application. The display quality for an 800x600 resolution LCD is dependant on the compromises that can be made between the LCD refresh rate and the application.

A full explanation of the graphics controller operation can be found in the PXA255 data sheets included on the support CD.

The flat panel data and control signals are routed to PL3. See the section PL3 – LCD connector, page 62, for pin assignment and part number details.

The VIPER-FPIF1 allows the user to easily wire-up a new panel using pin and crimp style connectors. Contact Arcom (see Appendix A – Contacting Arcom, page 72) for purchasing information.

A list of proven Flat Panel displays are included on the VIPER product page. Click on the *Flat Panel Display Options* tab for up-to-date details.

The following tables provide a cross-reference between the flat panel data signals and their function when configured for different displays.

TFT panel data bit mapping to the VIPER

Panel data bus bit	18-bit TFT	12-bit TFT	9-bit TFT
FPD 15	R5	R3	R2
FPD 14	R4	R2	R1
FPD 13	R3	R1	R0
FPD 12	R2	R0	NA
FPD 11	R1	NA	NA
GND	R0	NA	NA
FPD 10	G5	G3	G2
FPD 9	G4	G2	G1

Panel data bus bit	18-bit TFT	12-bit TFT	9-bit TFT
FPD 8	G3	G1	G0
FPD 7	G2	G0	NA
FPD 6	G1	NA	NA
FPD 5	G0	NA	NA
FPD 4	B5	B3	B2
FPD 3	B4	B2	B1
FPD 2	B3	B1	B0
FPD 1	B2	B0	NA
FPD 0	B1	NA	NA
GND	B0	NA	NA

The PXA255 cannot directly interface to 18-bit displays, as its color palette RAM has 5 bits of red, 6 bits of green, and 5 bits of blue, since the human eye can distinguish more shades of green than of red or blue.

STN panel data bit mapping to the VIPER

Panel data bus Bit	Dual scan color STN	Single scan color STN	Dual scan mono STN
FPD 15	DL6(G)	NA	NA
FPD 14	DL6(R)	NA	NA
FPD 13	DL5(B)	NA	NA
FPD 12	DL4(G)	NA	NA
FPD 11	DL3(R)	NA	NA
FPD 10	DL2(B)	NA	NA
FPD 9	DL1(G)	NA	NA
FPD 8	DL0(R)	NA	NA
FPD 7	DU7(G)	D7(G)	DL3
FPD 6	DU6(R)	D6(R)	DL2
FPD 5	DU5(B)	D5(B)	DL1
FPD 4	DU4(G)	D4(G)	DL0
FPD 3	DU3(R)	D3(R)	DU3
FPD 2	DU2(B)	D2(B)	DU2
FPD 1	DU1(G)	D1(G)	DU1
FPD 0	DU0(R)	D0(R)	DU0

Below is a table covering the clock signals required for passive and active type displays:

VIPER	Active display signal (TFT)	Passive display signal (STN)
PCLK	Clock	Pixel Clock
LCLK	Horizontal Sync	Line Clock
FCLK	Vertical Sync	Frame Clock
BIAS	DE (Data Enable)	Bias

The display signals are +3.3V compatible; the VIPER contains power control circuitry for the flat panel logic supply and backlight supply. The flat panel logic is supplied with a switched 3.3V (default) or 5V supply while the backlight is supplied with a switched 5V supply for the inverter.

There is no on-board protection for these switched supplies! Care must be taken during power up/down to ensure the panel is not damaged due to the input signals being incorrectly configured.

Typically the power up sequence is as follows (please check the datasheet for the particular panel in use):

1. Enable display VCC
2. Enable flat panel interface
3. Enable backlight

Power down is in reverse order.

LCD backlight enable

The PXA255 GPIO9 pin controls the LCD Inverter supply voltage for the backlight. When GPIO9 is set to logic ‘1’, the backlight supply BLKSAFE is supplied with 5V (turned on). The BLKEN signal on PL3 is the un-buffered GPIO9 signal. See the section PL3 – LCD connector, page 62, for PL3 pin assignment, connector and mating connector details.

If you want to use a 12V backlight inverter, then the switched 5V supply on BLKSAFE or the control signal BLKEN can be used to control an external 12V supply to the inverter.

LCD logic supply enable

The PXA255 GPIO10 pin controls the supply voltage for the LCD Logic. When GPIO10 is set to logic '1', the LCD supply LCDSAFE is supplied with 3.3V (turned on). See the section PL3 – LCD connector, page 62, for PL3 pin assignment, connector and mating connector details.

This may be factory configured (using a surface mount resistor) to supply 5V. If the flat panel logic is powered from 5V, it must be compatible with 3.3V signaling.

LCD backlight brightness control

The control of the backlight brightness is dependant upon the type of backlight inverter used in the display. Some inverters have a 'DIM' function, which uses a logic level to choose between two levels of intensity. If this is the case then GPIO16 (Alternative Function 0) is used to set this. Other inverters have an input suitable for a pulse-width modulated signal; in this case GPIO16 should be configured as PWM0 (Alternative Function 2).

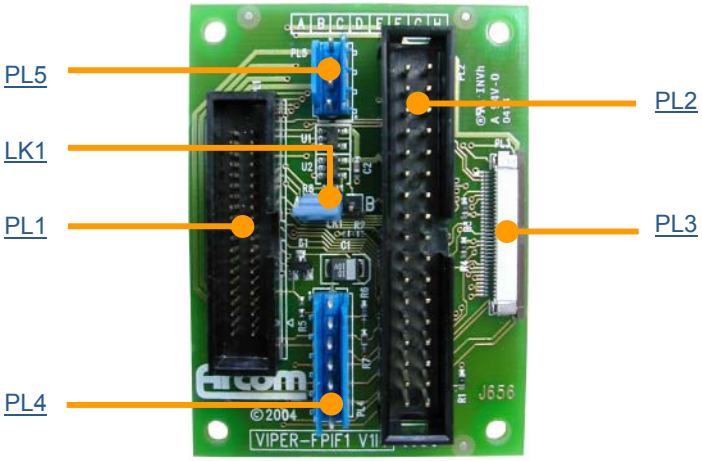
STN BIAS voltage

The VIPER provides a negative and a positive bias voltage for STN type displays. The negative and positive bias voltages are set to –22V and +22.5V respectively. Pin connections for these can be found in the section PL3 – LCD connector, page 62. Please contact Arcom for details of other bias voltages. Contact details are provided in Appendix A – Contacting Arcom, page 72.

Do not exceed 20mA load current.

VIPER-FPIF1 details

The VIPER-FPIF1 allows easy connection between the VIPER and a TFT or STN LCD flat panel display.



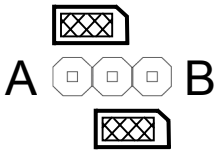
The connectors on the following pages are shown in the same orientation as the picture above.

Connector	Function
LK1	TFT Clock Delay Selection
PL1	Connects to the VIPER
PL2	Generic LCD Connector
PL3	Direct connection to a NEC NL3224BC35-20 5.5inch 320x240 TFT Display
PL4	Connects to Backlight Inverter
PL5	STN Bias Voltages

VIPER-FPIF1 Connectors

LK1 – TFT Clock Delay Selection

It has been found that some TFT displays require a delay on the clock, if this is required fit the jumper in position A, if not then fit in position B.

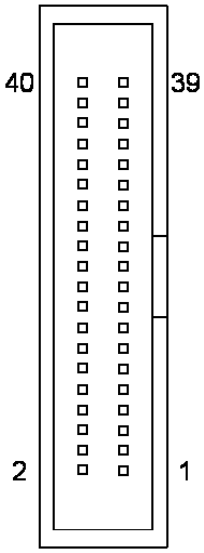


PL1 – VIPER LCD cable connector

Connector: Oupiin 3215-40GSB, 40-way, 1.27mm (0.05”) x 2.54mm (0.1”) straight-boxed header.

Mating connector: Oupiin 1203-40GB.

Pin	Signal Name	Pin	Signal Name
1	BLKEN#	2	BLKSAFE
3	GND	4	GND
5	NEGBIAS	6	LCDSAFE
7	GPIO16/PWM0	8	POSBIAS
9	GND	10	GND
11	BLUE_DATA0	12	BLUE_DATA1
13	BLUE_DATA2	14	BLUE_DATA3
15	GND	16	GND
17	BLUE_DATA4	18	GREEN_DATA0
19	GREEN_DATA1	20	GREEN_DATA2
21	GND	22	GND
23	GREEN_DATA3	24	GREEN_DATA4
25	GREEN_DATA5	26	FPD11
27	GND	28	GND
29	FPD12	30	FPD13
31	FPD14	32	FPD15
33	GND	34	GND
35	FCLK	36	BIAS / DE
37	GND	38	GND
39	PCLK	40	LCLK



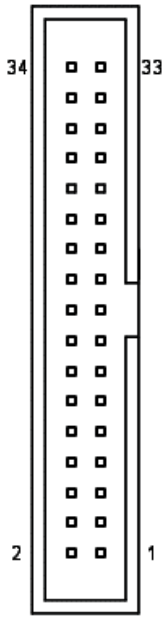
PL2 – Generic LCD connector

Connector: Taicom TI34BHS, 34-way, 2.54mm (0.1”) x 2.54mm (0.1”) straight-boxed header.

Mating connector: Fujitsu FCN-723-B034/2.

Mating connector crimps: Fujitsu FCN-723J-AU/Q. (As it is possible to connect a crimp type connector to PL2, a wide range of LCD displays can be connected with a custom cable.)

Pin	Signal Name	Pin	Signal Name
1	GND	2	BLUE_DATA0
3	BLUE_DATA1	4	BLUE_DATA2
5	GND	6	BLUE_DATA3
7	BLUE_DATA4	8	GREEN_DATA0
9	GREEN_DATA1	10	GND
11	GREEN_DATA2	12	GREEN_DATA3
13	GREEN_DATA4	14	GREEN_DATA5
15	GND	16	GND
17	RED_DATA0	18	RED_DATA1
19	RED_DATA2	20	GND
21	RED_DATA3	22	RED_DATA4
23	GND	24	PCLK
25	GND	26	LCDSAFE
27	LCDSAFE	28	LCLK
29	FCLK	30	GND
31	BKLSAFE	32	LBIAS
33	NC	34	BKLEN#

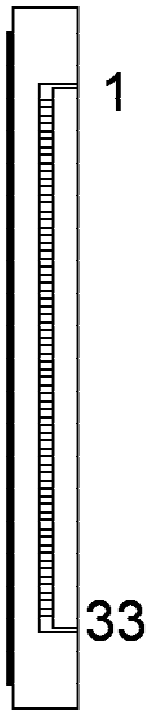


PL3 – Direct connection to a NEC NL3224BC35-20 5.5inch 320x240 TFT display

Connector: Oupiin 2345-33TD2.

Mating Cable: Eunsung 0.5x33x190xAx0.035x0.3x5x5x10x10.

Pin	Signal Name	Pin	Signal Name
1	PCLK	18	GREEN_DATA5
2	LCLK	19	GND
3	FCLK	20	GND
4	FCLK	21	BLUE_DATA0
5	GND	22	BLUE_DATA1
6	GND	23	BLUE_DATA2
7	RED_DATA0	24	BLUE_DATA3
8	RED_DATA1	25	BLUE_DATA4
9	RED_DATA2	26	GND
10	RED_DATA3	27	LBIAS
11	RED_DATA4	28	LCDSAFE
12	GND	29	LCDSAFE
13	GREEN_DATA0	30	GND
14	GREEN_DATA1	31	GND
15	GREEN_DATA2	32	GND
16	GREEN_DATA3	33	GND
17	GREEN_DATA4		

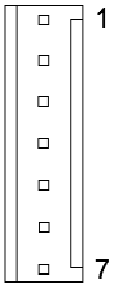


PL4 – Backlight inverter connector

Connector: Framatome 76384-407.

Mating Connector: Framatome 65240-007.

Pin	Signal Name
1	GND
2	PWM0
3	BKLEN#
4	GND
5	GND
6	BKLSAFE
7	BKLSAFE

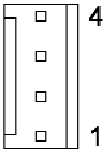


PL5 – STN Bias connector

Connector: Framatome 76384-404.

Mating Connector: Framatome 65240-004.

Pin	Signal Name
1	NEGBIAS
2	GND
3	GND
4	POSBIAS



Audio

A National Semiconductor LM4548A AC'97 audio CODEC is used to support the audio features of the VIPER. Audio inputs supported by the LM4548A are stereo line in and a mono microphone input.

The LM4548A provides a stereo line out that can also be amplified by a National Semiconductor LM4880 250mW per channel power amplifier, suitable for driving an 8Ω load. The LM4548A AC'97 codec may be turned off if it is not required. See the section Audio power management, page 58, for details.

Connection to the VIPER Audio features is via header PL6. See the table below for pin assignments and the section PL6 – Audio connector, page 65, for connector and mating connector details.

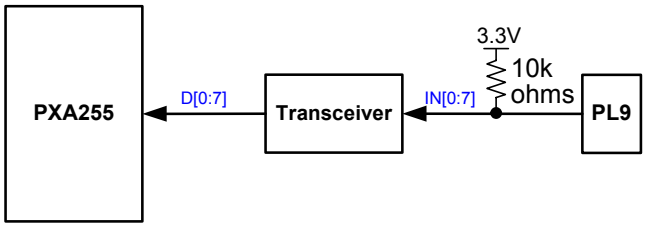
Function	Pin	Signal	Signal levels (max)
Microphone	10	MIC	1Vrms input
	7	Audio ground reference.	
Line in	1	Line input left	1Vrms input
	5	Line input right	
	3	Audio ground reference	
Line out	2	Line output left	1Vrms output
	6	Line output right	
	4	Audio ground reference	
Amp out	8	Amp output left	1.79Vpeak output, 1.26Vrms output (8Ω load) 223mW
	11	Amp output right	
	12	Audio ground reference	

General purpose I/O

Eight general-purpose input lines and eight general-purpose output lines are provided on connector PL9.

To read from IN[0:7], read the least significant byte from offset 0x500000 of CS5 (0x14500000) to sample the 8 inputs from PL9.

VIPER Inputs	PXA255 data
IN0	D0
IN1	D1
IN2	D2
IN3	D3
IN4	D4
IN5	D5
IN6	D6
IN7	D7



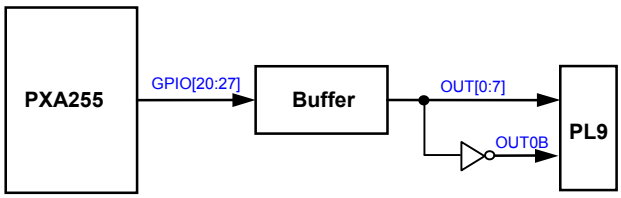
The PXA255 is not designed to interface to 8-bit peripherals, so when the 8-bits of data are read only the least significant byte from the word contains the data.

Data bus

Most Significant Byte								Least Significant Byte							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Don't Care								IN Data							

To write to OUT[0:7], write to the following PXA255 processor GPIO lines to drive the outputs.

VIPER Outputs	PXA255 GPIO
OUT0	GPIO20
OUT1	GPIO21
OUT2	GPIO22
OUT3	GPIO23
OUT4	GPIO24
OUT5	GPIO25
OUT6	GPIO26
OUT7	GPIO27



The PXA255 GPIO lines must be configured using the registers built into the device to ensure they function correctly. RedBoot configures GPIO20 – GPIO27 as outputs, and sets OUT0 – 2 to logic ‘0’, and OUT3 – 7 as logic ‘1’. Eboot cannot set these up as outputs as it only boots the Windows CE .NET image. Once Windows CE .NET is booted you can simply write to a mapped address. For an example of how to do this under Windows CE .NET please see the Windows CE .NET Technical Manual.

Please note:

- IN0-7 cannot be configured as outputs as they are hardwired as input-only by a buffer.
- OUT0-7 cannot be configured as inputs as they are hardwired as output-only by a buffer.

The GPIO lines are programmed using the GPCR0 and the GPSR0 to set the line to ‘0’ or ‘1’ respectively. The registers are 32-bit wide and bits 20-27 relate to GP20-27.

Register	Address
GPCR0	0x40E00024
GPSR0	0x40E00018

The general-purpose inputs are 5V tolerant, and the outputs can sink and source up to 24mA @ 3.3V.

OUT0B is an inverted OUT0 signal, and is driven to 5V, which provides compatibility with the VIPER-UPS.

The following general purpose IO lines are used by the VIPER-UPS:

Function	IO
External Power Fail	IN0
Battery Low	IN1
UPS Power down	OUT0B

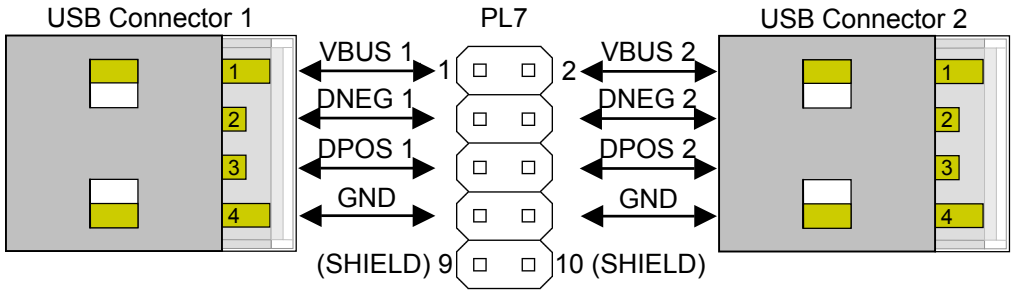
USB interface

There are two USB interfaces on the VIPER. These interfaces have been designed to support the Open Host Controller Interface (OpenHCI).

There are four signal lines associated with each USB channel:

- VBUS
- DPOS
- DNEG
- GND

Their arrangement is summarized in the following illustration:



A USB power control switch controls the power and protects against short-circuit conditions. See the section USB power management, page 58, for details of control.

If the USB voltage is short-circuited, or more than 500mA is drawn from either supply, the switch turns off the power supply and automatically protects the device and board. The VBUS power supply is derived from the VIPER +5V supply.

If you require details for the USB bus, or would like to determine whether particular peripherals are available, see www.usb.org.

A factory fit option changes USB port 1 from a host interface to a device using the PXA255 USB controller. Please contact Arcom for more details. Contact details are provided in Appendix A – Contacting Arcom, page 72.

10/100BaseTX Ethernet

An SMSC LAN91C111 Ethernet controller provides a single 10/100BaseTX interface. The device provides an embedded PHY and MAC, and complies with the IEEE802.3u 10/100BaseTX and IEEE 802.3x Full-duplex Flow Control specifications. Configuration data and MAC information are stored in an external 93C46 EEPROM.

The 10/100base-T magnetics are located on the VIPER. Connection to the VIPER Ethernet port is via header PL1. See PL1 – 10/100BaseTX Ethernet connector, page 61, for pin assignment, connector and mating connector details.

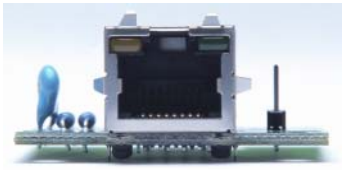
A second header PL2 provides the Activity and Link status LED signals. The output lines sink current when switched on therefore the anode of each LED should be connected to pins 1 and 3 of PL2 and the cathode to the appropriate status line.

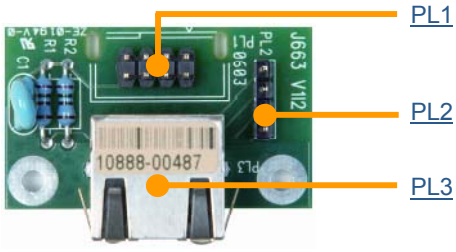
The Link LED illuminates when a 10 or 100base-T link is made, and the Activity LED illuminates when there is Tx or Rx activity.

Ethernet breakout board

Arcom can provide an Ethernet breakout board with an RJ45 connector to interface to the VIPER Ethernet connectors PL1 and PL2. The Ethernet breakout board features brackets for panel mounting ease.

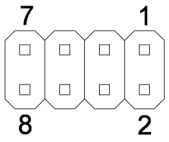
The Ethernet Breakout board allows easy connection between the VIPER and a 10/100base-T Ethernet Connection. It is shown below:



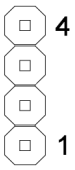


The connectors on the following pages are shown in the same orientation as the picture above.

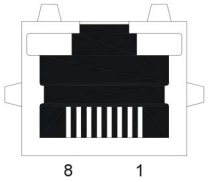
Connector	Function
PL1	10/100BaseTX Ethernet Signals
PL2	Ethernet LEDs
PL3	RJ45 Connector



Ethernet breakout PL1



Ethernet breakout PL2



Ethernet breakout PL3

Ethernet signal mapping between VIPER and Ethernet breakout connectors

Ethernet breakout PL1 – 2x4-way header		Ethernet breakout PL3 - RJ45		VIPER PL1 – 10/100BaseTX Ethernet connector	
Pin	**Signal Name**	**Pin**	**Signal Name**	**Pin**	**Signal Name**
1	Tx+	1	Tx+	1	Tx+
2	TX-	2	TX-	2	TX-
3	RX+	3	RX+	3	RX+
4	RJ-2	4	RJ-2	4	RJ-2
5	RJ-2	5	RJ-2	5	RJ-2
6	RX-	6	RX-	6	RX-
7	RJ-1	7	RJ-1	7	RJ-1
8	LANGND	8	RJ-1	8	LANGND

Ethernet LED signal mapping between VIPER and Ethernet breakout connectors

Ethernet breakout PL2 – 1x 4-way header		VIPER PL2 – Ethernet status LED's connector	
Pin	**Signal Name**	**Pin**	**Signal Name**
1	LINK LED+	1	3.3V
2	LINK LED-	2	LINK (Green)
3	ACTIVITY LED+	3	3.3V
4	ACTIVITY LED-	4	ACTIVITY (Yellow)
		5	NC
		6	NC

Serial COMs ports

There are five high-speed, fully functionally compatible 16550 serial UARTs on the VIPER. Four of these channels can be used as standard RS232 serial interfaces, and the remaining one (COM5) can be configured as RS422 or RS485.

Port	Address	IRQ	FIFO Depth RX / TX	Signals
COM1	0x40100000 – 0x40100023	Internal	64 / 64	RS232 Rx, Tx, CTS, RTS, RI, DSR, DCD, DTR
COM2	0x40200000 – 0x40200023	Internal	64 / 64	RS232 Rx, Tx, RTS, CTS
COM3	0x40700000 – 0x40700023	Internal	64 / 64	RS232 Rx, Tx
COM4	0x14300010 – 0x1430001F	GPIO3	128 / 128	RS232 Rx, Tx, CTS, RTS, RI, DSR, DCD, DTR
COM5	0x14300000 – 0x1430000F	GPIO4	128 / 128	RS422 / RS485 Tx, Rx

Please see the Intel Developer's Manual for details of internal interrupts.

COM1 – RS232 interface

Uses the Full Function UART in the PXA255 (FFUART). The port is buffered to RS232 levels by a 5V transceiver with ±15kV ESD protection, and supports full handshaking and modem control signals. Maximum baud rate on this channel is 230kb/s (this is limited by the transceiver performance). A factory fit option configures COM1 as TTL Level signals to interface to a modem. Please contact Arcom for details. Contact details are provided in Appendix A – Contacting Arcom, page 72.

COM2 – RS232 interface

Uses the Bluetooth UART in the PXA255 (BTUART). The port is buffered to RS232 levels by a 5V transceiver with ±15kV ESD protection, and supports RTS, CTS handshaking only. Maximum baud rate on this channel is 230kb/s (this is limited by the transceiver performance).

COM3 – RS232 interface

Uses the Standard UART in the PXA255 (STUART). The port is buffered to RS232 levels by a 5V transceiver with ±15kV ESD protection, but does not support any handshaking (RX / TX only). Maximum baud rate on this channel is 230kb/s (this is limited by the transceiver performance).

COM4 – RS232 interface

Supported on Channel 0 of an external Exar XR16C2852 with 128bytes of Tx and Rx FIFOs, and buffered to RS232 levels by a 5V transceiver with ±15kV ESD protection. The maximum baud rate on this channel is 115kb/s.

COM5 – RS422/485 interface

Supported on Channel 1 of an external Exar XR16C2852 with 128bytes of Tx and Rx FIFOs, and buffered to RS422/485 levels by a 5V transceiver with ±15kV ESD protection, to provide support for RS422 (default) and RS485 (jumper selectable) interfaces. The maximum baud rate on this channel is 115kb/s.

RS422

The RS422 interface provides full-duplex communication. The signals available are TXA, TXB, RXA, RXB and Ground. The maximum cable length for an RS422 system is 4000ft (1200m) and supports 1 transmitter and up to 10 receivers.

To enable RS422 operation, LK6 and LK7 should be in position ‘B’. LK4 and LK5 should be made if the board is at the end of the network. See RS485/422 configuration – LK4, LK5, LK6 and LK7, page 71, for details.

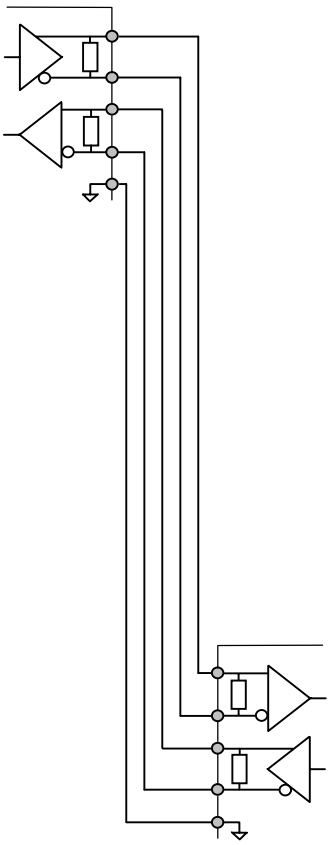
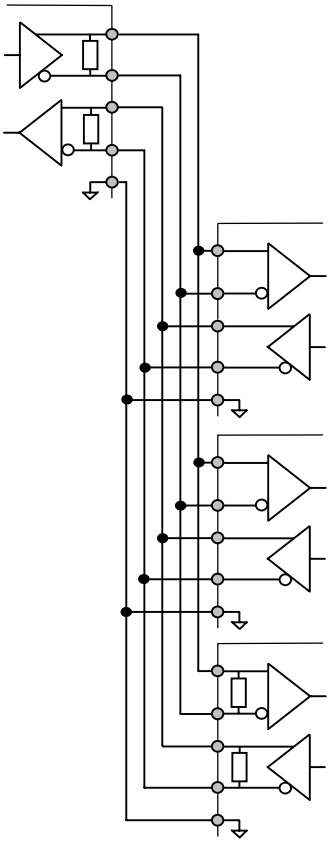
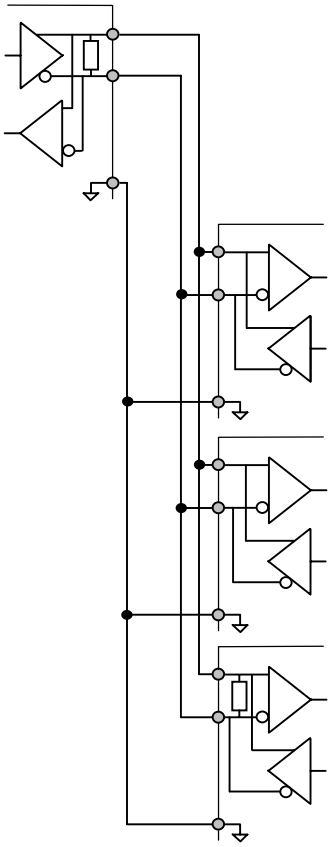
RS485

This is a half-duplex interface that provides combined TX and RX signals. PL4 pin 5 provides TXB/RXB and pin 6 provides TXA/RXA. A ground connection is also required for this interface. The maximum cable length for this interface is the same as RS422 (4000ft), but RS485 supports up to 32 transmitters and receivers on a single network. Only one transmitter should be switched on at a time.

The VIPER uses the RTS signal to control transmission. When this signal is at logic ‘1’ the driver is switched off and data can be received from other devices. When the RTS line is at logic ‘0’ the driver is on. Any data that is transmitted from the VIPER is automatically echoed back to the receiver. This enables the serial communications software to detect that all data has been sent and disable the transmitter when required. LK6 and LK7 should be in position ‘A’ to enable the RS485 interface. The UART used on the VIPER for COM5 has extended features including auto-RTS control for RS485. This forces the RTS signal to change state (and therefore the direction of the RS485 transceivers) when the last bit of a character has been sent onto the wire. Please refer to the XR16C2852 datasheet on the Development Kit CD.

LK4 and LK5 provide parallel line termination resistors and should be made if the VIPER is at the end of the network.

Typical RS422 and RS485 Connection

RS422 POINT-TO-POINT	RS422 MULTI-DROP	RS485 MULTI-DROP
		
Number of Wires 5 **Transmitters Enabled** always **Receivers Enabled** always **Duplex Mode** full **LK6** **B** **LK7** **B**	**Number of Wires** 5 **Transmitters Enabled** active RTS **Receivers Enabled** always **Duplex Mode** full **LK6** **B** **LK7** **B**	**Number of Wires** 3 **Transmitters Enabled** active RTS **Receivers Enabled** always **Duplex Mode** half **LK6** **A** **LK7** **A**

PC/104 interface

The PC/104 interface supports 8/16 bit ISA bus style signals. Add on boards can be used to enhance the functionality of the main board. Arcom has an extensive range of PC/104 compliant modules and these can be used to quickly add digital I/O, analog I/O, serial ports, video capture devices, PC card interfaces etc. The ISA bus is based on the x86 architecture and is not normally associated with RISC processors. It shall be necessary to modify standard drivers to support any 3rd party PC/104 modules.

Any PC/104 board plugged in will appear in the PC Card memory space socket 1.

Address	Region Name
0x3D000000 – 0x3FFFFFFF	Reserved
0x3C000000 – 0x3CFFFFFF	PC/104 memory space (16MB)
0x30000400 – 0x3BFFFFFF	Reserved
0x30000000 – 0x300003FF	PC/104 I/O space (1kB)

The PC/104 bus signals are compatible with the ISA bus electrical timing definitions. DMA, bus mastering, and shared interrupts are not supported on the VIPER's PC/104 interface. For details on PC/104 Interrupts please see PC/104 interrupts, page 26.

The VIPER provides +5V to a PC/104 add-on-board via the PL11 and PL12 connectors. If a PC/104 add-on-board requires a +12V supply, then +12V must be supplied to the VIPER power connector PL16 pin 4. If –12V or –5V are required, these must be supplied directly to the PC/104 add-on board.

All signals between the PXA255 and the PC/104 are buffered. When access to the PC/104 bus is not in use the PXA255 socket 1 and the PC/104 connector are automatically isolated by the buffers transceiver output enables being driven to '1'.

JTAG and debug access

Debug access to the PXA255 400MHz XScale processor is via the JTAG connector PL10 and the reset pin of PL17. The EPI Majic^{MX} probe has been used to debug the PXA255 processor on the VIPER. There are many other debug tools that can be interfaced to the VIPER for access to the JTAG Interface of the Intel XScale PXA255 processor.

The tables below detail the pins connections between the VIPER and Majic^{MX}.

Compare PL10 and PL17 pin numbers to match VIPER JTAG connection to the Majic^{MX} connections.

VIPER JTAG Connections

Connector	Pin	Name	Description
PL10	1	VCC3	3.3V Supply pin to JTAG debug tool
	3	GND	Ground reference
	3	GND	Not required on VIPER.
	4	nTRST	PXA255 JTAG interface reset
	6	TDI	JTAG test data input to the PXA255
	7	TDO	JTAG test data output from the PXA255
	8	TMS	PXA255 JTAG test mode select
	9	TCK	PXA255 JTAG test clock
PL17	6	RESETSW	System reset
	-	-	-
	-	-	Not required on VIPER
	-	-	Not supported by VIPER

Majic^{MX} Connections

Connector	Pin	Name	Description
PL10	1	VTRef	JTAG interface voltage reference for Majic^{MX}
	3	GND	Ground reference
	3	RTCLK	Ground to stop RTCLK from floating.
	4	nTRST	Majic^{MX} JTAG interface reset
	6	TDI	JTAG test data output from the Majic^{MX}
	7	TDO	JTAG test data input to the Majic^{MX}
	8	TMS	Majic^{MX} JTAG test mode select
	9	TCK	Majic^{MX} JTAG test clock
PL17	6	nSRST	Open collector system reset
	-	VSupply	Not used
	-	DBGREQ	Never used
	-	DBGACK	Used for tracing with MAJIC^{PLUS} passive probe

The Majic^{MX} probe supports industry-standard debugger APIs, such GNU gdb for Linux and Microsoft Platform Builder for Windows CE .NET, which allows you to choose the EPI debugger or a wide variety of other third party debuggers.

Power and power management

Power supplies

The VIPER is designed to operate from a single +5V ±5% (4.75V to +5.25V) supply. The power connector PL16 has a +12V connection defined, but is not required for the VIPER under normal operation. It can be used to supply +12V to the PC/104 stack if required. For details of the power connector please see the section PL16 – Power connector, page 68.

There are four on board supply voltages derived from the +5V supply. These are +1.06 to +1.3V (microprocessor Core), +1.8V (CPLD Core) and two +3.3V. One of the +3.3V supplies is dedicated for use with the CompactFLASH interface on PL5 and +3.3V flat panels on PL3.

The +5V supply is monitored automatically on-board; if this supply falls below +4.63V the board is reset. When the power supply rises above this threshold voltage the board comes out of reset and reboots itself. The power supply monitor ensures that the board does not hang if the supply voltage fails at any point.

If using the CompactFLASH socket and an LCD display, ensure the total current requirement on 3.3V does not exceed 900mA! Please check the datasheets of the devices you are using, as there is no on-board protection!

Battery backup

An external battery (CR2032 or similar) providing +3.0V to +3.3V can be used as a battery backup for the DS1307 RTC and the SRAM. The external battery supplies power to the battery backup circuit only when there is no +5V supply to the board.

To use an external battery connect its + and - terminals across PL16 pins 3 (VBAT) and 2 (GND) respectively, see PL16 – Power connector, page 68.

The table below shows the typical and maximum current load on the external battery.

Device Load on Battery	Typical (µA)	Maximum (µA)
SRAM	0.2	2
DS1307 RTC with Clock Out Off	0.3	0.5
DS1307 RTC with Clock Out On	0.48	0.8
Supply Supervisor	0.6	1
Total with RTC Clock Out Off	**1.1**	**3.5**
Total with RTC Clock Out On	**1.28**	**3.8**

An onboard Schottky diode drops 13mV from VBAT at 25°C. At -40°C this may increase to 170mV and at +85°C decrease below 10mV. The SRAM and DS1307 minimum voltages are 1.5V and 2V respectively. If the supply falls below these points then the corresponding device may loose data. Please check your battery datasheet for mAh and operating temperature specifications.

Power management

The VIPER board supports various power management functions. Under normal conditions the VIPER consumes typically 405mA ±5mA (2025mW ±25mW) once it has finished booting. During the boot process the VIPER consumes up to 470mA, 2350mW. This is with:

- The processor running at 400MHz in idle mode.
- Its external memory running at 100MHz.
- All on board peripherals powered.
- No external peripherals powered.

To estimate the power consumption of the VIPER use the following formula:

(VIPER current (norm) - processor current saving
- on board peripheral current saving + external peripheral current) x 5V

Read the following subsections to estimate the power for the processor, on board and external peripheral devices.

Processor power estimations

Take into account the processor operating frequency, core voltage and memory frequency for the application. The figures shown in the table below are when the processor memory frequency is set to 100MHz. Currently embedded Linux and VxWorks supports changing the operating frequency and Windows CE .NET will provide support shortly. Please refer to the relevant operating system technical manual to select an alternative operating frequency.

Processor Mode	Vcore (V)	Current Saving (mA) from 5V when Processor Core is				
		400MHz	300MHz	200MHz	100MHz	Asleep
Active	1.29	-92 ±15	-	-	-	-
Active	1.1	-	-46 ±15	-	-	-
Active	1.06	-	-	-31 ±15	-16 ±21	-
Idle	1.29	0 (default)	-	-	-	-
Idle	1.1	-	14	-	-	-
Idle	1.06	-	-	15	20	-
Sleep	1.06	-	-	-	-	62

Current figures when the microprocessor is active were taken with the following load conditions. Calculating checksums of two files (first file: 1.1MB and second file: 0.5MB), and copying two 256kB files.

On board peripheral device power estimations

Use the table below to estimate power savings from on board peripheral devices.

Ethernet Power down	COM1 – COM5 Sleep Mode	AC'97 Codec shutdown	Current Saving (mA)	Power Saving (mW)
-	-	Yes	54	270
-	Yes	-	59	295
-	Yes	Yes	113	565
Yes	-	-	123	615
Yes	-	Yes	177	885
Yes	Yes	-	182	910
Yes	Yes	Yes	236	1180

External peripheral device power estimations

Take into account any external peripherals by an application, such as:

- USB devices: Keyboard, Memory Stick, and Mouse.
- CompactFLASH socket: CompactFLASH memory, or Microdrive
- Flat Panel Display: TFT logic + backlight, STN logic + backlight + bias voltage

The table give examples of addition current / power from external peripheral devices.

Device	Part Number	Condition	Additional Current (mA)	Additional Power (mW)
32MB Sandisk CompactFLASH	SDCFB-32-101-80	Inserted, (no access)	1	5
		Reading consistently	48	240
64MB FlashDio™ USB memory stick	FDU100A	Inserted, (no access)	75	375
		Reading consistently	121	605
NEC 5.5" LCD + Inverter (as used with VIPER-ICE)	NL3224BC35-20 + 55PW131	LCD and backlight on	650	3250
		LCD on and backlight off	291	1455

For devices using the 3.3V supply from the CompactFLASH socket and FPD logic supply, use 92% as the regulator efficiency.

Power estimate examples

Example 1: VIPER in standby (microprocessor in sleep mode and every power saving option enabled)

In this case, the power consumed by the respective categories is:

- VIPER current (norm) = 405mA ±5mA
- Processor current saving = 62mA
- On board peripheral current saving = 236mA
- External peripheral current = 0mA

Applying the formula shown on page 52, the estimated VIPER current in standby is:

405mA ±5mA - 62mA - 236mA + 0mA
= 107mA ±5mA (535mW ±25mW).

Example 2: VIPER at 400MHz with 100MHz external memory + LCD with backlight on

In this case, the power consumed by the respective categories is:

- VIPER current (norm) = 405mA (tolerance accounted for in CPU current saving)
- Processor current saving = -92 ±15mA
- On board peripheral current saving = 0mA
- External peripheral current = +650mA

Therefore, the estimated current the VIPER is using is:

405mA + 92mA ±15mA - 0mA + 650mA
= 1147mA, ±15mA (5735mW, ±75mW).

Processor power management

The power manager in the PXA255 offers the ability to disable the clocks to the different internal peripherals. By default, all clocks are enabled after reset. To reduce power consumption disable the clocks for any unused peripherals.

The clock speed of the processor core, PXbus (the internal bus connecting the microprocessor core and the other blocks of the PXA255), LCD and SDRAM can also be changed to achieve a balance between performance and power consumption. For more details on the internal power manager please see the Intel PXA255 developer's manual on the Development Kit CD.

To adjust the core voltage, write the values shown in the following table to the LTC1659 DAC. Please see the LTC1659 datasheet and Intel® PXA255 Processor Electrical, Mechanical, and Thermal Specification on the Development Kit CD.

DAC Data Hex Value	CPU Core Voltage	Comment
0x000	1.65V	Not recommended to set the VCORE above 1.3V as the power consumption will increase for no performance benefit.
0x325	1.29V	Typical VCORE for peak voltage range at 400MHz operation. Maximum VCORE for medium voltage range at 200MHz operation.
0xDE5	1.1V	Typical VCORE for high voltage range at 300MHz operation.
0xFFF	1.06V	Typical VCORE for low voltage and medium voltage range, suitable for 100MHz to 200MHz operation.

When the microprocessor is in sleep mode, the CPU core voltage is shutdown.

To communicate with the VCORE DAC, use the following pins to emulate the LTC1659 interface:

GPIO	LTC1659 DAC pin Function
GPIO6	Data
GPIO11	⌐↑ Clock
GPIO19	Chip Select

Before putting the PXA255 into sleep mode, ensure that the R_DIS bit in the ICR register located at offset 0x100002 from CS5 (0x14100000) is set to '1'. The PXA255 is not designed to interface to 8-bit peripherals, so only the least significant byte from the word contains the data.

Interrupt configuration and reset register

Byte lane	Most Significant Byte								Least Significant Byte							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	-	-	-	-	-	-	-	R_DIS	AUTO_CLR	RETRIG
Reset	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0
R/W	-	-	-	-	-	-	-	-	W							
Address	0x14100002															

ICR bit functions

Bit	Name	Value	Function
0	RETRIG	0	No interrupt retrigger (embedded Linux/VxWorks)
		1	Interrupt retrigger (Windows CE .NET)
1	AUTO_CLR	0	No auto clear interrupt / toggle GPIO1 on new interrupt
		1	Auto clear interrupt / low pulse for 1.12µS on GPIO1 on new interrupt
2	R_DIS	0 1	Keep set as 0 under normal operating conditions.
3 - 7	-	X	No function

UART power management

COM4 and COM5 are generated from an external Exar XR16C2852 DUART. This device supports a sleep mode with an auto wake up. By enabling this feature the DUART enters sleep mode when there are no interrupts pending. The part resumes normal operation when any of the following occur:

- Receive data start bit.
- Change of state on: CTS, DSR, CD, RI
- Data is being loaded into transmit FIFO.

If the part is awakened by one of the above conditions, it returns to the sleep mode automatically after the condition has cleared. Please see the XR16C2852 datasheet on the Development Kit CD for information on enabling the sleep mode. Placing the XR16C2852 into low power mode can reduce the power consumption of the VIPER by 2mA (10mW).

GPIO12 and GPIO13 on the PXA255 can be used to power down the RS232 drivers on the VIPER, to save power. The following table shows the affect of GPIO12 and GPIO13 on the RS232 drivers. Placing the drivers in shutdown mode can reduce the power consumption of the VIPER by up to 57mA (285mW).

GPIO12	GPIO13	Operation Status	Transmitters	Receivers
0	0	Normal Operation	Active	Active
0	1	Receiver Disabled	Active	High-Z
1	X	Shutdown	High-Z	High-Z

CompactFLASH power management

The power supply to the CompactFLASH interface is controlled via software, and supports hot swap card insertion and CompactFLASH power down states. GPIO82 on the PXA255 is used to control the power supply. Setting this line to logic ‘0’ switches off power to the CompactFLASH interface.

Ethernet power management

The network interface supports a power down mode, which shuts down the internal MAC and PHY blocks of the network controller. Placing the controller into low power mode can reduce the power consumption of the VIPER by up to 123mA (615mW). To power down the PHY write ‘1’ to the power down bit in the MII PHY Register 0, Control Register. To power down the MAC write ‘1’ to the EPH PowerEN bit in the Bank 1, Configuration Register. See the LAN91C111 datasheet contained on the Development Kit CD for further details.

USB power management

The USB Host controller supports a USB suspend state. Placing the controller into the USB suspend state can reduce the power consumption of the VIPER by up to 21mA (105mW). To suspend the USB, the software must write to the relevant bits in the HcControl Register (81h). Please see the ISP1160 datasheet contained on the Development Kit CD.

Audio power management

The audio interface supports the AC'97 low power modes. Shutting down the digital and analog interfaces can reduce consumption by up to 54mA (270mW).

To shut down the AC'97 Codec, the software must write to the relevant bits in the Powerdown Control / Status Register (26h). Please see the LM4548A datasheet contained on the Development Kit CD.

Wake up events

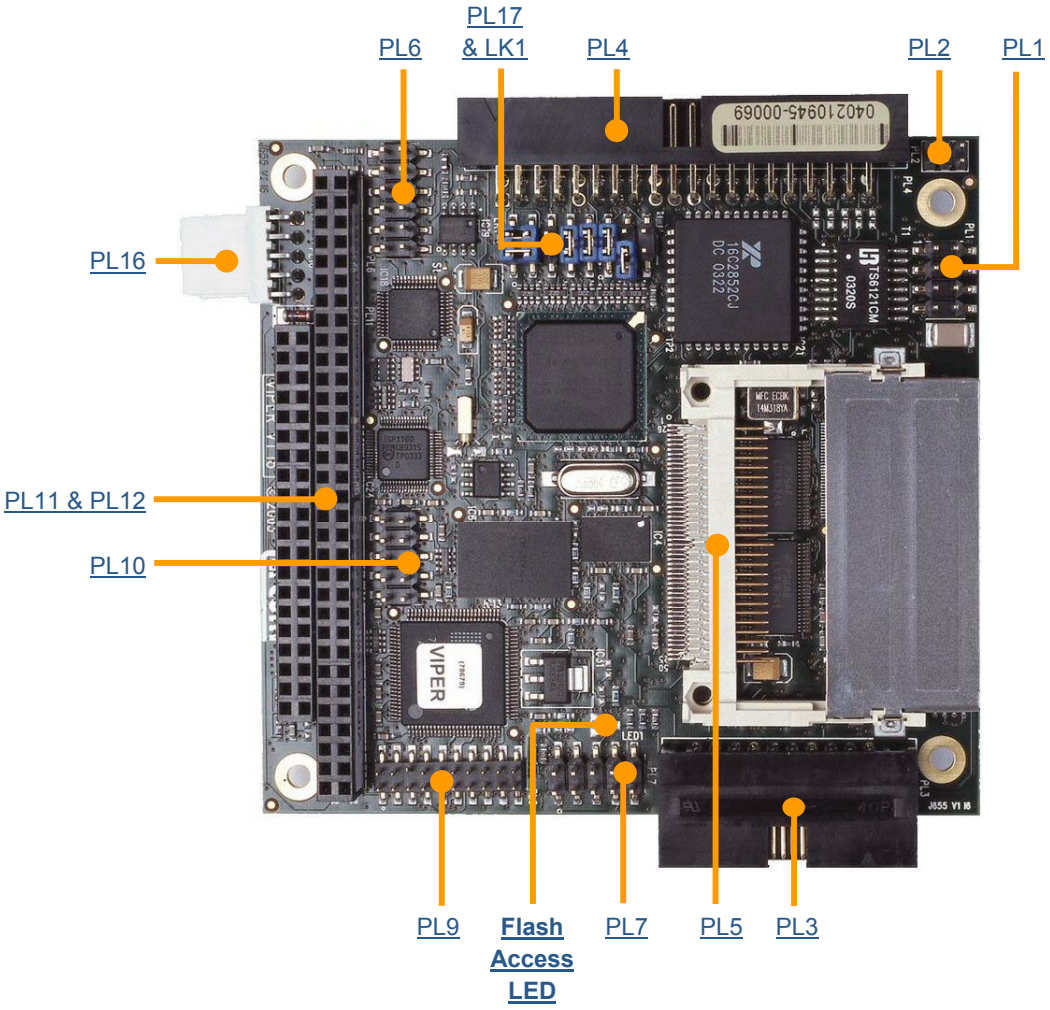
When the PXA255 processor is placed into sleep mode, a number of different sources can be used to wake the processor. Below is a list of sources, and the related PXA255 GPIO signal.

Source	GPIO
Ethernet	GPIO0
PC/104 IRQ	GPIO1
USB	GPIO2
COM5	GPIO3
COM4	GPIO4
RTC Alarm	Internal

See section 3.5 in the PXA255 Applications Processor Developers Manual, included in the Development Kit CD.

Connectors, LEDs and jumpers

The following diagram shows the location of the connectors, LEDs and jumpers on the VIPER:



The connectors on the following pages are shown in the same orientation as the picture above, unless otherwise stated.

Connectors

There are 12 connectors on the VIPER for accessing external devices.

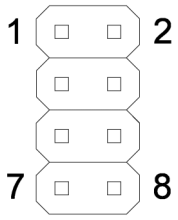
Connector	Function	Connector Details in Section
PL1	10/100BaseTX Ethernet interface	PL1 – 10/100BaseTX Ethernet connector, page 61
PL2	Ethernet controller status LED's	PL2 – Ethernet status LED's connector, page 61
PL3	LCD panel interface	PL3 – LCD connector, page 62
PL4	Serial Ports	PL4 – COMS ports, page 63
PL5	CompactFLASH type I/II	PL5 – CompactFLASH connector, page 64
PL6	Audio	PL6 – Audio connector, page 65
PL7	USB	PL7 – USB connector, page 65
PL9	GPIO	PL9 – GPIO connector, page 66
PL10	JTAG	PL10 – JTAG connector, page 66
PL11	64-way PC/104 expansion	PL11 & PL12 – PC/104 connectors, page 67
PL12	40-way PC/104 expansion	PL11 & PL12 – PC/104 connectors, page 67
PL13	Factory use only (no connector fitted)	-
PL16	Power / battery / external reset	PL16 – Power connector, page 68
PL17 & LK1	Link header	PL17 & LK1 – Jumper header, page 68

PL1 – 10/100BaseTX Ethernet connector

Connector: Oupiin 2015-2 X 4 G D, 8-way, 2.54mm (0.1”) x 2.54mm (0.1”) dual row header.

Mating connector: Framatome 71600-008.

Pin	Signal Name	Pin	Signal Name
1	TX+	2	TX-
3	RX+	4	RJ-2
5	RJ-2	6	RX-
7	RJ-1	8	LANGND



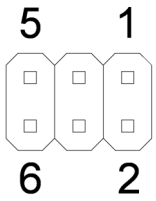
PL2 – Ethernet status LED's connector

Connector: Molex 87089-0616, 6-way, 2mm (0.079”) x 2mm (0.079”) pin header.

Mating connector: Molex 51110-0650.

Mating connector crimps (x6): Molex 50394-8100.

Pin	Signal Name	Pin	Signal Name
1	3.3V	2	Link
3	3.3V	4	Activity
5	NC	6	NC

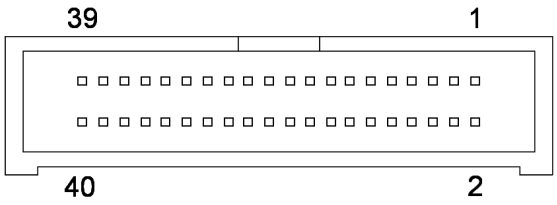


PL3 – LCD connector

Connector: Oupiin 3214-40GRB, 40-way, 1.27mm (0.05”) x 2.54mm (0.1”) right angled boxed header.

Mating connector: Oupiin 1203-40GB.

Pin	Signal Name	Pin	Signal Name
1	BLKEN#	2	BLKSAFE
3	GND	4	GND
5	NEGBIAS	6	LCDSAFE
7	GPIO16/PWM0	8	POSBIAS
9	GND	10	GND
11	FPD0	12	FPD1
13	FPD2	14	FPD3
15	GND	16	GND
17	FPD4	18	FPD5
19	FPD6	20	FPD7
21	GND	22	GND
23	FPD8	24	FPD9
25	FPD10	26	FPD11
27	GND	28	GND
29	FPD12	30	FPD13
31	FPD14	32	FPD15
33	GND	34	GND
35	FCLK	36	BIAS / DE
37	GND	38	GND
39	PCLK	40	LCLK



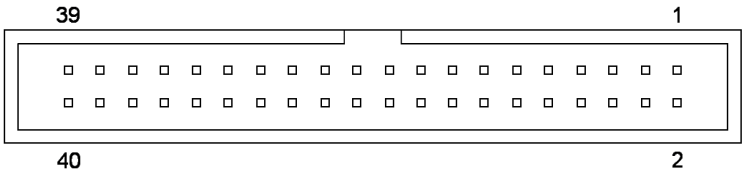
As viewed from the connector pins

PL4 – COMS ports

Connector: Oupiin 3014-40GRB, 40-way, 2.54mm (0.1”) x 2.54mm (0.1”) dual row IDC boxed header.

Mating connector: Framatome 71600-040.

Pin	Signal Name	Pin	Signal Name
1	NC	2	NC
3	NC	4	NC
5	TX5+ (RS422) (TX5+/RX5+ RS485)	6	TX5- (RS422) (TX5-/RX5- RS485)
7	RX5+ (RS422)	8	RX5- (RS422)
9	GND	10	GND
11	TX3	12	RX3
13	RX2	14	RTS2
15	TX2	16	CTS2
17	GND	18	GND
19	GND	20	NC
21	DCD4	22	DSR4
23	RX4	24	RTS4
25	TX4	26	CTS4
27	DTR4	28	RI4
29	GND	30	NC
31	DCD1	32	DSR1
33	RX1	34	RTS1
35	TX1	36	CTS1
37	DTR1	38	RI1
39	GND	40	NC

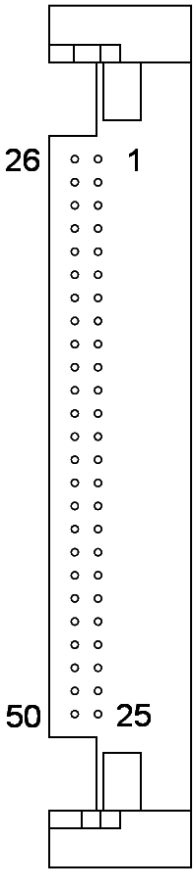


As viewed from the connector pins

PL5 – CompactFLASH connector

Connector: 3M N7E50-A516HE-50, 50-way CompactFLASH Type II Connector.

Pin	Signal Name	Pin	Signal Name
26	/CD1	1	GND
27	D11	2	D03
28	D12	3	D04
29	D13	4	D05
30	D14	5	D06
31	D15	6	D07
32	/CE2	7	/CE1
33	/VS1 (GND)	8	A10
34	/IORD	9	/OE
35	/IOWR	10	A09
36	/WE	11	A08
37	RDY/BSY	12	A07
38	+3.3V	13	+3.3V
39	GND	14	A06
40	N/C	15	A05
41	/RESET	16	A04
42	WAIT	17	A03
43	/INPACK (NU)	18	A02
44	/REG	19	A01
45	N/C	20	A00
46	N/C	21	D00
47	D08	22	D01
48	D09	23	D02
49	D10	24	/IOCS16
50	GND	25	/CD2

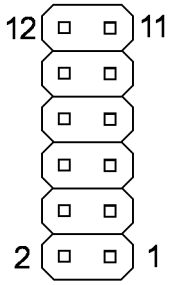


PL6 – Audio connector

Connector: Oupiin 2015-2 X 6 G D, 12-way, 2.54mm (0.1”) x 2.54mm (0.1”) dual row header.

Mating connector: Framatome 71600-012.

Pin	Signal Name	Pin	Signal Name
1	LEFT IN	2	LEFT OUT
3	GND	4	GND
5	RIGHT IN	6	RIGHT OUT
7	GND	8	AMP LEFT OUT
9	GND	10	MIC IN
11	AMP RIGHT OUT	12	GND

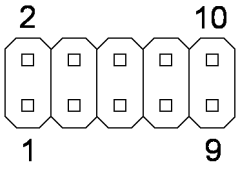


PL7 – USB connector

Connector: Oupiin 2015-2 X 5 G D, 10-way, 2.54mm (0.1”) x 2.54mm (0.1”) dual row header.

Mating connector: Framatome 71600-010.

Pin	Signal Name	Pin	Signal Name
1	VBUS-1	2	VBUS-2
3	DNEG-1	4	DNEG-2
5	DPOS-1	6	DPOS-2
7	GND	8	GND
9	SHIELD	10	SHIELD



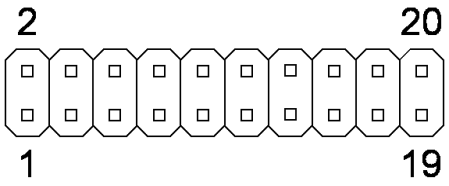
PL9 – GPIO connector

Connector: Oupiin 2115-2 X 10 G D N, 20-way, 2mm (0.079”) x 2mm (0.079”) dual row header.

Mating connector: Framatome 69307-020.

Mating connector crimps (x20): Framatome 77138-001.

Pin	Signal Name	Pin	Signal Name
1	+5V	2	+5V
3	IN0	4	IN1
5	IN2	6	IN3
7	IN4	8	IN5
9	IN6	10	IN7
11	OUT0	12	GND
13	OUT0_ INVERTED	14	OUT1
15	OUT2	16	OUT3
17	OUT4	18	OUT5
19	OUT6	20	OUT7

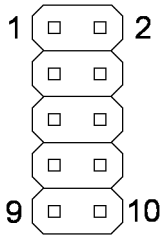


PL10 – JTAG connector

Connector: Oupiin 2015-2 X 5 G D, 10-way, 2.54mm (0.1”) x 2.54mm (0.1”) dual row header.

Mating connector: Framatome 71600-010.

Pin	Signal Name	Pin	Signal Name
1	VCC3	2	NC
3	GND	4	nTRST
5	NC	6	TDI
7	TDO	8	TMS
9	TCLK	10	NC

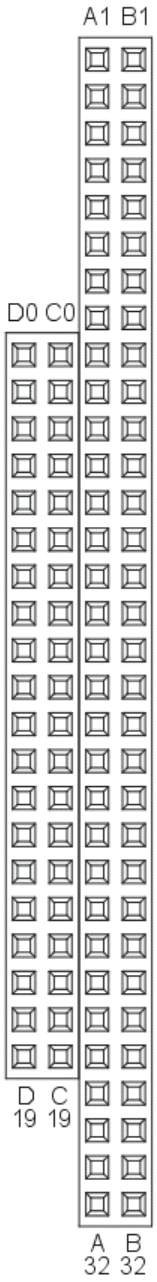


PL11 & PL12 – PC/104 connectors

Connectors:

- Astron 25-1201-232-2G, 64-way, 2.54mm (0.1”) x 2.54mm (0.1”) Stackthrough PC/104 compatible connector (row A & B).
- Astron 25-1201-220-2G, 40-way, 2.54mm (0.1”) x 2.54mm (0.1”) Stackthrough PC/104 compatible connector (row C & D).

PL12			PL11		
Pin	**Row D**	**Row C**	**Pin**	**Row A**	**Row B**
			1	/IOCHCK	GND
			2	D7	RSTDRV
			3	D6	+5V
			4	D5	NU (IRQ9)
			5	D4	NC
			6	D3	NU (DRQ2)
			7	D2	NC
			8	D1	NC
0	GND	GND	9	D0	+12V
1	/MEMCS16	/SBHE	10	IOCHRDY	KEY
2	/IOCS16	LA23	11	AEN	/SMEMW
3	IRQ10	LA22	12	A19	/SMEMR
4	IRQ11	LA21	13	A18	/IOW
5	IRQ12	LA20	14	A17	/IOR
6	NU (IRQ15)	LA19	15	A16	NU (DACK3)
7	NU (IRQ14)	LA18	16	A15	NU (DRQ3)
8	NU (DACK0)	LA17	17	A14	NU (DACK1)
9	NU (DRQ0)	/MEMR	18	A13	NU (DRQ1)
10	NU (DACK5)	/MEMW	19	A12	NU (REFSH)
11	NU (DRQ5)	D8	20	A11	8MHz Clk
12	NU (DACK6)	D9	21	A10	IRQ7
13	NU (DRQ6)	D10	22	A9	IRQ6
14	NU (DACK7)	D11	23	A8	IRQ5
15	NU (DRQ7)	D12	24	A7	IRQ4
16	+5V	D13	25	A6	IRQ3
17	NC (Master)	D14	26	A5	NU (DACK2)
18	GND	D15	27	A4	NU (TC)
19	GND	KEY	28	A3	BALE
			29	A2	+5V
			30	A1	OSC
			31	A0	GND
			32	GND	GND

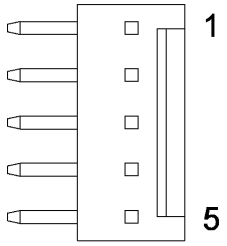


PL16 – Power connector

Connector: Molex 22-05-7058, 5-way, 2.54mm (0.1") Pitch KK® Header - Right Angle Friction Lock 7395 series connector.

Mating Connector: Molex 22-01-2055, 5-way, 2.54mm (0.1") Pitch KK® Crimp Terminal Housing 2695 series connector.

Pin	Signal Name
1	+5V
2	GND
3	VBAT
4	+12V
5	/Reset



VBAT provides connections for a battery backup supply for the 256KByte static RAM and the Dallas DS1307 64 x 8 Serial Real-Time Clock.

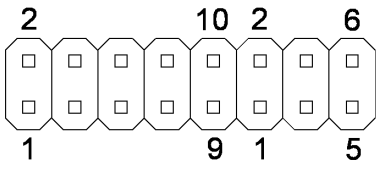
+12V connection defined, but is not required for the VIPER under normal operation. It can be used to supply +12V to the PC/104 stack if required.

A momentary switch (push to make) may be connected across /Reset and GND. Do not connect the switch across /Reset and +5V or +12V.

PL17 & LK1 – Jumper header

Connector: Oupiin 2015-2 X 8 G D, 16-way, 2.54mm (0.1”) x 2.54mm (0.1”) dual row header.

Ref	Pin	Signal Name	Pin	Signal Name
	6	RESETSW	5	GND
PL17	4	User Config 1	3	GND
	2	Reserved	1	GND
	10	RX5/TX5-_120R	9	PL4_RX5/TX5+
	8	RX5-_120R	7	PL4_RX5+
LK1	6	PL4_RX5/TX5+	5	PL4_RX5/TX5-
	4	RX5+	3	RX5-
	2	PL4_RX5+	1	PL4_RX5-



Status LED's

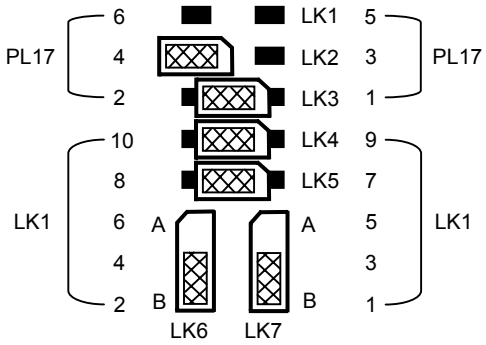
There is a single status LED on the VIPER, which indicates FLASH access to the bootloader FLASH or the main FLASH memory / Silicon Disk.

Jumpers

There are seven user selectable jumpers on the VIPER, their use is explained below.

Default settings

The default positions of the jumpers is as follows:



Rotate this diagram 90° clockwise to match the VIPER picture on page 59.

Reset – LK1

A momentary switch (push to make) may be connected to LK1. When the button is pressed the board goes into a full hardware reset. When the switch is released (open circuit) the board reboots.

User configurable jumper 1 – LK2

This jumper can be used by an application program to signify a configuration setting.

LK2	Description
	GPIO7 read as ‘0’.
	GPIO7 read as ‘1’.

Default setting:

Reserved – LK3

This jumper is reserved for factory use only.

RS485/422 configuration – LK4, LK5, LK6 and LK7

These jumpers are used to enable/disable the RS485 receive buffer and RS485/422 line termination, see COM5 – RS422/485 interface, page 46, for more details.

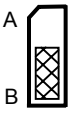
This jumper can be used by an application program to signify a configuration setting.

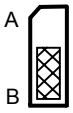
LK4	Description
	(RS485 TX/RX) RS422 TX line termination resistor (120Ω) connected.
	(RS485 TX/RX) RS422 TX line termination resistor (120Ω) disconnected.

Default setting: 

LK5	Description
	RS422 RX line termination resistor (120Ω) connected.
	RS422 RX line termination resistor (120Ω) disconnected.

Default setting: 

LK6 & LK7	Description
	RS485 half-duplex.
	RS422 full-duplex.

Default setting: 

Only fit LK4 and LK5 if the VIPER is at the end of the network.

Appendix A – Contacting Arcom

Arcom sales

Arcom's sales team is always available to assist you in choosing the board that best meets your requirements. Contact your local sales office or hotline.

Sales office US

Arcom
7500W 161st Street
Overland Park
Kansas
66085
USA

Tel: 913 549 1000
Fax: 913 549 1002
E-mail: us-sales@arcom.com

Sales office Europe

Arcom
Clifton Road
Cambridge
CB1 7EA
UK

Tel: 01223 411 200
Fax: 01223 410 457
E-mail: euro-sales@arcom.com

Full information about all Arcom products is available on our Web site at www.arcom.com.

While Arcom's sales team can assist you in making your decision, the final choice of boards or systems is solely and wholly the responsibility of the buyer. Arcom's entire liability in respect of the boards or systems is as set out in Arcom's standard terms and conditions of sale. If you intend to write your own low level software, you can start with the source code on the disk supplied. This is example code only to illustrate use on Arcom's products. It has not been commercially tested. No warranty is made in respect of this code and Arcom shall incur no liability whatsoever or howsoever arising from any use made of the code.

Technical support

Arcom has a team of technical support engineers who can provide assistance if you have any problems with your VIPER board.

Technical support US

Tel: 913 549 1010
Fax: 913 549 1001
E-mail: us-support@arcom.com

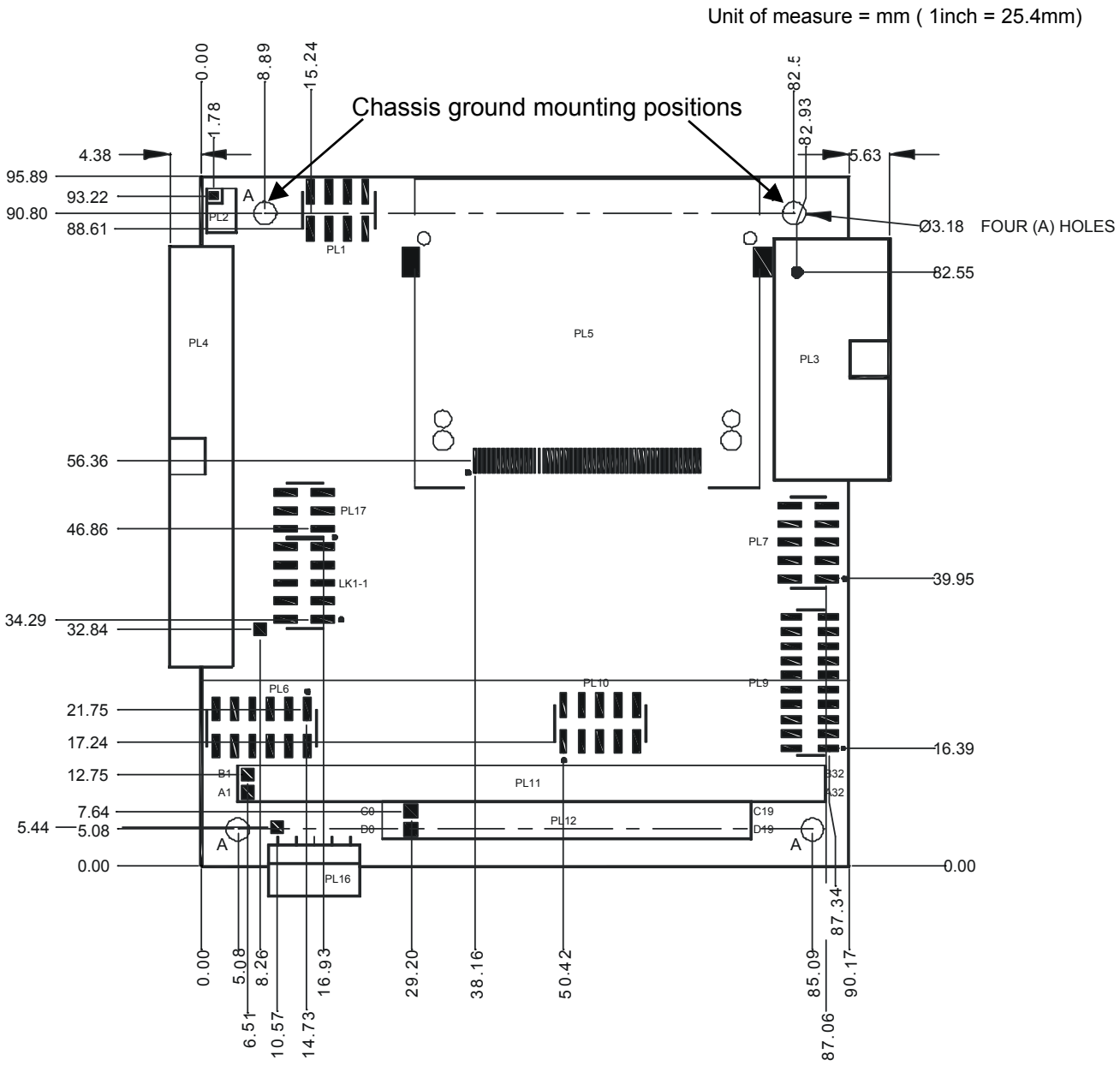
Technical support Europe

Tel: +44 (0)1223 412 428
Fax: +44 (0)1223 403 409
E-mail: euro-support@arcom.com

Appendix B – Specification

Microprocessor	Intel XScale™ PXA255 processor.	
Memory	16MByte, 64MByte 3.3V un-buffered SDRAM. 16MByte, 32MByte Intel StrataFLASH. 1MByte Bootloader ROM. 256k SRAM (battery backed off board).	
Graphics Controller	PXA255 Flat panel controller offering resolutions: • 320 x 240, 8/16 bpp. • 640 x 480, 8/16 bpp. • 800 x 600, 8 bpp.	
Peripherals	Serial:	RS232 on COM1, COM2, COM3, & COM4 RS422/485 on COM5.
	CompactFLASH:	One 50 pin Type I/II CompactFLASH Socket.
	Audio:	16-bit AC'97-compliant CODEC, stereo.
	USB:	Dual channel v1.1 host support (factory fit device option).
Temperature	Operating:	-20°C (-4°F) to +70°C (+158°F) (commercial). -40°C (-40°F) to +85°C (+185°F) (industrial).
Humidity	10% to 90% RH (non-condensing).	
Real Time Clock	Accuracy +/- 1 minute/month.	
Software	RedBoot Bootloader for embedded Linux or VxWorks. Eboot Bootloader for Windows CE .NET.	
Power Requirement	5V +/- 5%. 2W typical consumption (without LCD, CF or USB devices fitted). 107mA ±5mA (535mW ±25mW) in standby mode.	
Battery Input	2.7v to 3.3v (external). Typical discharge 2μA.	
Dimensions	PC/104 compatible format. 3.775" x 3.550". 96mm x 91mm.	
Weight	96 grams.	
MTBF	90,000 hours based on MIL-HDBK-217F using generic failure rates.	

Appendix C - Mechanical diagram



When mounting the VIPER use only M3 (metric) or 4-40 (US) screws. The mounting pad is 6.35mm, 0.25” and the hole is 3.175mm, 0.125”, so ensure any washers fitted are smaller than the pad.

Using oversized screws and washers, or tooth locking washers, can cause short circuits and over-voltage conditions.

We recommend that you use a Loctite screw thread lock or a similar product over tooth locking washers

Appendix D - Reference information

Product information

Product notices, updated drivers, support material, 24hr-online ordering:

www.arcom.com

PC/104 Consortium

PC/104 Specifications. Vendor information and available add on products.

www.PC/104.org

USB Information

Universal Serial Bus (USB) Specification and product information

www.usb.org

CFA (CompactFlash Association)

CF+ and CompactFlash Specification and product information

http://www.compactflash.org

Intel

Intel XScale™ PXA255 processor documentation

www.intel.com

http://www.intel.com/design/pca/prodbref/252780.htm

Standard Microsystems Corporation

SMSC SMC91C111 Ethernet Controller documentation

www.smsc.com

Exar Corporation

Exar XR16C2852 DUART with 128Byte FIFO documentation

www.exar.com

National Semiconductor Corporation

National Semiconductor LM4548A AC'97 Codec documentation

http://www.national.com

Koninklijke Philips Electronics N.V.

Philips LM4548A AC'97 Codec documentation

http://www.philips.com

Maxim Integrated Products Inc.

Maxim DS1307 64 x 8 Serial Real Time Clock documentation

http://www.maxim-ic.com

Linear Technology Corporation.

Linear Technology LTC1659 Micropower DAC documentation

http://www.linear.com/

Appendix E - Acronyms and Abbreviations

API	Application Program(ming) Interface
BTUART	Bluetooth UART
CFI	Common FLASH Interface
CODEC	Coder/Decoder
COM	Communication Port
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit (PXA255)
CMOS	Complementary Metal Oxide Semiconductor
DMA	Direct Memory Access
EEPROM	Electrically Erasable and Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EPROM	Erasable and Programmable Read-Only Memory
FFUART	Full Function UART
FIFO	First-In First-Out
FPIF1	Flat Panel Interface
GPIO	General Purpose Input/Output
ICE	In-Circuit-Emulator
IO	Input/Output
LED	Light Emitting Diode
LCD	Liquid Crystal Display
LSB	Least Significant Bit
NA	Not Applicable
NC	No Connect
NU	Not Used
NiMH	Nickel Metal Hydride
OS	Operating System
PROM	Programmable Read-Only Memory
PWM	Pulse-Width Modulation
QVGA	Quarter VGA, display resolution 320 x 240 pixels
REF DES	Reference Designator, Component Identification Number on the PCB
RTC	Real Time Clock
SBC	Single Board Computer
SDRAM	Synchronous Dynamic Random Access Memory
SRAM	Static Random Access Memory
STN	Super Twisted Nematic, technology of passive matrix liquid crystal
STUART	Standard UART
TFT	Thin Film Transistor, a type of LCD flat-panel display screen
UART	Universal Asynchronous Receiver / Transmitter
UPS	Uninterruptible Power Supply
USB	Universal Serial Bus
VAC	Voltage Alternating Current
VDC	Voltage Direct Current
VGA	Video Graphics Adapter, display resolution 640 x 480 pixels
VIPER-ICE	VIPER-Industrial Compact Enclosure

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